IRPS
International Reliability Physics Symposium

2022 IEEE International Reliability Physics Symposium (IRPS)

March 27-31, 2022

Dallas, Texas

IRPS 2022 General Chair Welcome Message

Welcome to IRPS 2022! When the IRPS Management Committee began making plans for Dallas, we recognized the strong desire by the reliability physics community to return to a face-to-face symposium that we last had in Monterey in 2019. But as time progressed, we recognized that travel restrictions were not being lifted as rapidly as we anticipated. Rather than leave out those of you who could not attend in person, we adopted a hybrid format allowing for both remote attendance and remote presentations. This is a first for IRPS and I am confident it will be a success for all.

With this new hybrid format, the symposium will return to the original five-day format with Tutorials and Year in Review on the first two days. The Technical Program, Keynote Talks, Workshops and Poster session will be held on the following three days. All of these (except Workshops and Posters) will be available via real-time streaming in the US Central Time zone with virtual attendees having Q&A access to the presenters. For those virtual attendees who cannot watch the live presentations, the material will be available on demand to all attendees for a month after the symposium with the ability to communicate with the authors.

In 2020, we were planning on co-hosting the International ESD Workshop (IEW) ESD workshop when the COVID-19 pandemic hit. For 2022, IEW will be seamlessly embedded into the IRPS Program and will sponsor three tutorials, an invited talk, two technical sessions and two evening workshops focused on ESD and latch-up. And we continue our collaboration with our sister conference, European Symposium on Reliability of Electron Devices Failure Physics and Analysis (ESREF) by hosting their Best Paper and the International Integrated Reliability Workshop (IIRW) by hosting their Best Student Paper.

Our primary objective is to maintain the symposium's leadership role in the reliability physics of microelectronic devices by attracting leading researchers to present their work and providing attendees the best place to access this information. With all the buzz in the media about whether Moore's Law has hit its limit, IRPS has been promoting expertise developed in silicon-based reliability over the past sixty years and expanding into new material areas. This year, eight of the technical sessions are devoted to reliability in topics outside of traditional silicon, including wide bandgap GaN/SiC, emerging memory and neuromorphic computing. I hope our ability to draw these communities together will accelerate the cross-fertilization of ideas.

The Technical Program consists of four keynote speakers, twenty-three invited speakers and eighty-seven oral presentations organized in thirty technical sessions on eighteen reliability topics. Over two evenings, there will be ten Workshops and sixty-six Poster presentations that are designed to allow in person attendees and experts to interact with one another. With eighteen tutorials covering topics ranging from fundamental transistor and memory reliability all the way up to automotive and complex system-level reliability, this year's symposium provides an excellent learning opportunity for engineers and scientists new to reliability as well as experienced individuals wanting to explore new areas. The Year in Review, which serves as a summary of research in the past year, will cover 3D packaging, emerging memory and aging aware circuit designs.

Finally, I would like to express my extreme gratitude to our patrons and exhibitors, whose support makes IRPS possible. And to all of you, our in person and virtual attendees, for supporting this symposium for sixty years!

Charles W. Slayman, General Chair

of 2022 IRPS Management Committee

2022 IEEE International Reliability Physics Symposium - *Tutorial & Year-in-Review Program*

March 27-31 | Dallas, Texas, USA

All Times in Central Daylight Time (CDT)

Sunday • March 27

Time	Min	International I & II	International III & IV
		TUT 1	TUT2
10:30 AM	90	Interaction of HCI, BTI and TDDB *Xavier Fiederspiel, ST*	Failure Analysis and its Relationship to Reliability and Product Quality *George Gaut, Qualcomm*
12:00 PM	60	Lunch (60 Min) - Windfall	
		TUT3	TUT4
1:00 PM	90	Transition Metal Dichalcogenides: Processing, Scaling, Performance, and Reliability *Chris Hinkle,* *University of Notre Dame*	Mechanical Effects in BEOL *Gavin Hall, Infineon*
2:30 PM	30	Break (30 Min) - International Foyer	
		TUT 5	TUT 6
3:00 PM	90	Telemetry and Machine Learning Enabled Health Management of Compute Systems *Nikhil Vichare, Dell*	3D interconnect reliability – A status *Stéphane Moreau, CEA-LETI*
4:30 PM		Adjourn	

Monday • March 28

Time	Min	International I & II	International III & IV	Cap Rock I, II & III	Becker I & II
		TUT 7	TUT 8	TUT 9	TUT 10
8:30 AM	90	A Common Physical Framework for CMOS Front End Reliability - BTI, HCD and TDDB *Souvik Mahapatra, IITB*	GaN Power Devices: Challenges for Improved Stability and Reliability *Matteo Meneghini,* *University of Padova*	Flash Memory Reliability and Error Mitigation in Modern SSDs *Nikolaos Papandreou &* *Haralampos Pozidis, IBM*	Advanced CMOS Technology challenges for robust ESD Design *Shih-Hung Chen, IMEC*
10:00 AM	30	Break (30 Min) - International Foyer			
		TUT 11	TUT 12	TUT 13	TUT 14
10:30 AM	90	RF/mmW/5G Reliability *Sriram Kalpat, Qualcomm*	Defects in SiC Epilayers on Device Yield and Reliability *Bob Stahlbush,* *Navy Research Lab*	PCM (Phase Change Memory) Reliability *Wanki Kim &* *Richard Southwick, IBM*	SOC ESD Design and Verification *Hanz Kunz, TI*
12:00 PM	60	Lunch (60 Min) - Windfall			
		TUT 15	TUT 16	TUT 17	TUT 18
1:00 PM	90	High-density Electronic Circuits Made of 2D Materials: Towards Their Integration in CMOS Silicon Chips *Mario Lanza, KAUST*	Automotive Use Conditions—Trends & Reliability Challenges *Jyotika Athavale, Nvidia*	Probabilistic Design for Reliability of Microelectronic and Photonic Materials, Devices, Packages and Systems *Ephraim Suhir,* *Portland State University*	Analog ESD Design Integration Challenges *Raj Sankaralingam, TI*
2:30 PM	30	Break (30 Min) - International Foyer			
		International III & IV			
3:00 PM	50	YIR 1: 3D IC Packaging *Kangwook (Kriss) Lee, SK hynix*			
3:50 PM	50	YIR 2: Emerging Memory Reliability (MRAM, RRAM, PCM) *Shimeng Yu, Georgia Tech*			
4:40 PM	50	YIR 3: Reliability and Aging Aware Designs / Circuit Reliability *Evelyn Landman, proteanTecs*			
5:30 PM		Adjourn			

2022 IEEE International Reliability Physics Symposium - *Technical Program*

March 27-31 | Dallas, Texas, USA

All Times in Central Daylight Time (CDT)

Tuesday • March 29

Time	Min	International III & IV		
8:00 AM	15	General Chair: Welcome & Introduction		
8:15 AM	10	Program Chair: Overview of Technical Program		
8:25 AM	10	Awards		
8:35 AM	45	Keynote 1: M. Alavi *(Intel)*		
9:20 AM	45	Keynote 2: S. Krishnamoorthy *(Synopsys)*		
10:05 AM	20	Break (20 Min)		
		Int. I & II	Int. III & IV	Cap Rock I, II & III
10:25 AM	5	2A - GD	2B - GaN	2C - SR
10:30 AM	25	2A.1	2B.1	2C.1
10:55 AM	25	2A.2	2B.2	2C.2
11:20 AM	25	2A.3	2B.3	2C.3
11:45 AM	25	2A.4	2B.4	2C.4
12:10 PM	20	Authors' Corner / Break - International Foyer		
12:30 PM	60	Lunch (60 min) - Windfall		
1:30 PM	5	3A - RT	3B - WB	3C - NC
1:35 PM	25	3A.1	3B.1	3C.1
2:00 PM	25	3A.2	3B.2	3C.2
2:25 PM	25	3A.3	3B.3	3C.3
2:50 PM	25	3A.4	3B.4	3C.4
3:15 PM	20	Authors' Corner / Break - International Foyer		
3:35 PM	5	4A - EM	4B - RF	4C - PK
3:40 PM	25	4A.1	4B.1	4C.1
4:05 PM	25	4A.2	4B.2	4C.2
4:30 PM	25	4A.3	4B.3	4C.3
4:55 PM	25	4A.4	4B.4	4C.4
5:20 PM	25		4B.5	4C.5
5:45 PM	20	Authors' Corner		
6:05 PM		Adjourn		

6:05 PM	55	Workshop Reception - Bonnie & Clyde Pavilion
7:00 PM	55	Workshops 1-5
7:55 PM	10	Break - International Foyer
8:05 PM	55	Workshops 6-10

**Workshops available to on-site attendees only*

Wednesday • March 30

Time	Min	International III & IV		
8:00 AM	45	Keynote 3: N. Chandrasekaran *(Micron)*		
8:45 AM	20	Break (20 Min) - International Foyer		
		Int. I & II	Int. III & IV	Cap Rock I, II & III
9:05 AM	5	5A - PI	5B - WB	5C - EL
9:10 AM	25	5A.1	5B.1	5C.1
9:35 AM	25	5A.2	5B.2	5C.2
10:00 AM	25	5A.3	5B.3	5C.3
10:25 AM	20	Authors' Corner / Break - International Foyer		
10:45 AM	5	6A - TX	6B - MR	6C - EL
10:50 AM	25	6A.1	6B.1	6C.1
11:15 AM	25	6A.2	6B.2	6C.2
11:40 AM	25	6A.3	6B.3	
12:05 PM	20	Authors' Corner / Break - International Foyer		
12:25 PM	60	Lunch (60 min) - Windfall		
1:25 PM	5	7A - RT	7B - MR	7C - SE
1:30 PM	25	7A.1	7B.1	7C.1
1:55 PM	25	7A.2	7B.2	7C.2
2:20 PM	25	7A.3		7C.3
2:45 PM	20	Authors' Corner / Break - International Foyer		
3:05 PM	5	8A - PR	8B - WB	8C - MB
3:10 PM	25	8A.1	8B.1	8C.1
3:35 PM	25	8A.2	8B.2	8C.2
4:00 PM	25	8A.3	8B.3	8C.3
4:25 PM	25	8A.4	8B.4 - IIRW BSP	8C.4
4:50 PM	25	8A.5	8B.5 - ESREF BP	
5:15 PM	20	Authors' Corner		
5:35 PM		Adjourn		

6:00 PM	180	6:00-9:00 PM Taste of Texas Poster Dinner Austin Ranch

*Invited Speaker

Thursday • March 31

Time	Min	International III & IV		
8:00 AM	45	Keynote 4: J. He *(TSMC)*		
8:45 AM	20	Break (20 Min) - International Foyer		
		Int. I & II	Int. III & IV	Cap Rock I, II & III
9:05 AM	5	9A - PR	9B - RT	9C - NC
9:10 AM	25	9A.1	9B.1	9C.1
9:35 AM	25	9A.2	9B.2	9C.2
10:00 AM	25	9A.3	9B.3	9C.3
10:25 AM	20	Authors' Corner / Break - International Foyer		
10:45 AM	5	10A - TX	10B - GaN	10C - FA
10:50 AM	25	10A.1	10B.1	10C.1
11:15 AM	25	10A.2	10B.2	10C.2
11:40 AM	25	10A.3	10B.3	10C.3
12:05 PM	25	10A.4 - LN	10B.4	10C.4
12:30 PM	20	Authors' Corner / Break - International Foyer		
12:50 PM	60	Lunch (60 min) - Windfall		
1:50 PM	5	11A - GD	11B - RF	11C - CR
1:55 PM	25	11A.1	11B.1	11C.1
2:20 PM	25	11A.2	11B.2	11C.2
2:45 PM	25	11A.3	11B.3	11C.3
3:10 PM	25	11A.4	11B.4	11C.4
3:35 PM	25	11A.5 - LN	11B.5	
4:00 PM	20	Authors' Corner / Break - International Foyer		
		International III & IV		
4:20 PM	15	Closing Ceremony, Prize Drawing & 2023 Introduction		
4:35 PM		Adjourn		

CR - Circuit Reliability and Aging	PK - Packaging & 2.5/3D Assembly
EM - Emerging Memory	PI - Process Integration
EL - ESD and Latchup	PR - Product Reliability
FA - Failure Analysis	RT - Reliability Testing
GaN - GaN Power Device	RF - RF/mmW/5G
GD - Gate/MOL Dielectrics	SE - Soft Errors
MR - Memory Reliability	SR - System Electronics Reliability
MB - Metal./BEOL Reliability	TX - Transistors
NC - Neuromorphic Comput. Rel.	WB - Wide-Bandgap Semi. (SiC)

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   2022 IEEE International Reliability Physics Symposium

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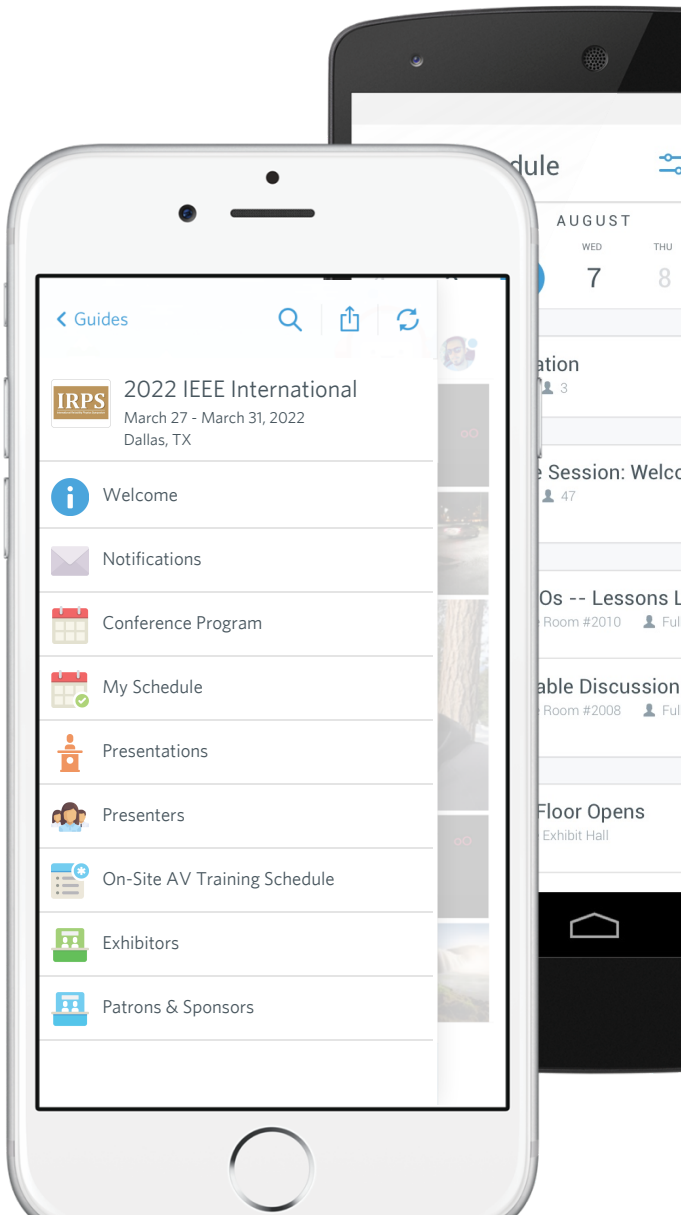

2022 IEEE International Reliability Physics Symposium (IRPS 2022)

Sunday, March 27

Tutorial 1
Sunday, March 27, 10:30 a.m. – 12:00 p.m. CDT
Venue: International I & II

10:30 a.m.
TuT1 (Tutorial) - Interaction of HCI, BTI and TDDB, Xavier Federspiel; Stmicroelectronics

Wear-out mechanisms in CMOS device (TDDB, BTI, HCI) have been extensively characterized in many detailed aspects, including voltage dependencies, time power law, channel length dependencies and relaxation. Particularly for HCI, several defect generation mechanisms have been evidenced (single or multiple particle defect generation process). Modeling of wear-out mechanisms have successfully been implemented in circuit simulators to predict wear-out resulting from circuit wave forms. Except for BTI contribution to Pfet HCI, aging models are, in general, modeled and implemented as independent mechanisms. Our purpose here is to present a methodology to investigate interactions between wear-out mechanisms. We will investigate if defect generation process corresponding to different wearout mechanisms are simultaneous but independent or in competition with each other's such as for the case of "age" concept. We will present results across technologies, to investigate interaction between various HCI modes, between NBTI and HCI, "off-state" and HCI as well as for TDDB and HCI. Finally, conclusions will be drawn with respect to circuit simulation implementation.

Tutorial 2
Sunday, March 27, 10:30 a.m. – 12:00 p.m. CDT
Venue: International III & IV

10:30 a.m.
TuT2 (Tutorial) - Failure Analysis and its Relationship to Reliability and Product Quality, George Gaut; Qualcomm

This tutorial is intended to show those Failure Analysis (FA) tools that would be most appropriate for the analysis of the specific reliability stress being performed. Each reliability stress typically has a specific objective to determine the product survivability over time from a package or die perspective. It will show the FA tool capabilities and weaknesses with respect to what is being stressed. The plan is to show the variety of each tool type by different manufactures. The intent is to also show the general costs associated with each tool type and an estimate of analysis time by tool.

Break
Sunday, March 27, 12:00 p.m. – 01:00 p.m. CDT

Tutorial 3
Sunday, March 27, 01:00 p.m. – 02:30 p.m. CDT
Venue: International I & II

01:00 p.m.
TuT3 (Tutorial) - Transition Metal Dichalcogenides: Processing, Scaling, Performance, and Reliability, Chris Hinkle; University of Notre Dame

Two-dimensional materials offer unique opportunities in nanoelectronic devices including stacked nanosheet transistors, back-end-of-line access devices, liners for scaled interconnects, and magnetic memory devices. While some impressive device performances have been demonstrated in recent years utilizing transition metal dichalcogenides (TMDs), the overall progress has been underwhelming compared to expectations. This tutorial will discuss the state-of-the-art in TMD synthesis, device strategies and performance, and reliability. Challenges with realizing large-area thin films, defect reduction and mitigation, gate stack (EOT) scaling, doping, and contact resistance will be addressed with correlations to device performance illustrated. By the end, we will provide a path forward for improved material and device quality, variability, and reliability including a benchmarked assessment of specific device technologies in which 2D materials will provide superior performance.

Tutorial 4
Sunday, March 27, 01:00 p.m. – 02:30 p.m. CDT
Venue: International III & IV

01:00 p.m.
TuT4 (Tutorial) - Mechanical Effects in BEOL, Gavin Hall; Infineon

Back-end-of-line (BEOL) reliability is characterized by several intrinsic tests including electromigration, stress migration, thermal cycling, and power cycling tests. What these tests have in common is the use of large mechanical stress loadings, either directly or indirectly, to accelerate failure in the metallization, barriers and/or surrounding dielectric. Test methodology, test structure design, along with the materials used, are key to the selection of intrinsic reliability models and their applicability to use conditions. As scaling proceeds, it is ever more important also to understand extrinsic size effects – e.g. linewidths, metal density and networks, grain boundaries, twins, and texture - and how these relate to stress and the inelastic response. These topics will be treated in this tutorial under the general guiding thread of the mechanics of failure—from the theory to practical application. Finally, we will discuss the relevant diagnostic and physical/electrical failure analysis techniques, experimental design, and analysis of statistical data for understanding and predicting the reliability of BEOL.

Break
Sunday, March 27, 02:30 p.m. – 03:00 p.m. CDT

Tutorial 5
Sunday, March 27, 03:00 p.m. – 04:30 p.m. CDT
Venue: International I & II

03:00 p.m.
TuT5 (Tutorial) - Health Management of Systems using Telemetry & Machine Learning, Nikhil Vichare; Dell

Methods that combine telemetry data from sensors with inference derived from Machine Learning models have been widely used for diagnostics, failure prediction, and health / performance personalization of systems. This tutorial will introduce the various strategies utilized for comprehensive health management of complex systems. The talk will highlight the various challenges pertaining to data collection, labeling, class imbalance, etc. that are often unique to training Machine/Deep learning models for fault detection and failure prediction. Mathematical techniques and engineering solutions to overcome some of these challenges will be presented. The tutorial will briefly cover methods and strategies for deploying and managing the life cycle of models embedded on client devices as well as those hosted on the cloud. Although the tutorial will use examples from computer systems to guide the discussion, the methods and approaches presented are applicable to a wide variety of applications.

Tutorial 6
Sunday, March 27, 03:00 p.m. – 04:30 p.m. CDT
Venue: International III & IV

03:00 p.m.
TuT6 (Tutorial) - 3D Interconnect Reliability – A Status, Stéphane Moreau; CEA-Leti

3D integration technologies have emerged less than 10 years ago as viable solutions for meeting IC requirements such as higher performance, increased functionality, lower power consumption, and a smaller footprint. Some examples of 3D integration in products are CMOS Image Sensors (CIS), memories and interposers. Through-Silicon-Vias (TSVs) are integrated in most of these products, because they allow die-level assembly, and simplify some aspects of test and packaging. However, TSVs disadvantage is the Keep Out Zones (KOZs) combined with a Cu pillar pitch typically limited to 20-40 μm. For some applications, such as CMOS image sensors and memories, smaller pitches (< 10 μm) are required for the vertical die-to-die connections; direct hybrid bonding (HB) is the solution of interest. While the first HB products are put on the market few studies are published with data about robustness/reliability. This tutorial will give you an overview of the reliability threats faced by TSVs and hybrid bonding-based interconnects after an introduction to the world of reliability and accelerated life tests.

Monday, March 28

Tutorial 7
Monday, March 28, 08:30 a.m. – 10:00 a.m. CDT
Venue: International I & II

08:30 a.m.
TuT7 (Tutorial) - A Common Physical Framework for CMOS Front End Reliability - BTI, HCD and TDDB, Souvik Mahapatra; Indian Institute of Technology Bombay

Several experimental features of Bias Temperature Instability (BTI), Hot Carrier Degradation (HCD) and Time Dependent Dielectric Breakdown (TDDB) in MOSFET are explained by a common physical framework. The framework calculates the kinetics of trap generation at the channel/gate insulator interface and inside the gate insulator bulk of a MOSFET, using a generalized Reaction-Diffusion-Drift (RDD) model. The reaction phase governs the bias and temperature dependence of trap generation, and is triggered by channel cold carriers for BTI, channel hot carriers for HCD and anode hole injection for TDDB. This is followed by diffusion of molecular and drift of ionic Hydrogen (or related) species that govern the time kinetics (power-law slope) of generated traps. Charge trapping in pre-existing traps, when necessary, is calculated by the Activated Barrier Double Well Thermionic (ABDWT) model. The following features are modeled: * BTI stress and recovery kinetics, gate bias and temperature dependence, impact of SiGe channel (for PMOS), Nitrogen in the gate stack and mechanical strain due to layout and device dimensional scaling. * HCD stress kinetics and different power-law time slopes, drain bias dependence, impact of technology scaling, involving shift of bell shape to monotonic gate bias dependence and negative to positive temperature dependence. * TDDB, impact of oxide thickness scaling on voltage acceleration factor and Weibull slope. The trap generation and trapping framework is incorporated into a commercial technology CAD (TCAD) tool to enable simulation of 3D devices (FinFETs, GAA FETs), which also includes effects due to quantum confinement, mechanical strain and self heating.

Tutorial 8
Monday, March 28, 08:30 a.m. – 10:00 a.m. CDT
Venue: International III & IV

08:30 a.m.
TuT8 (Tutorial) - GaN Power Devices: Challenges for Improved Stability and Reliability, Matteo Meneghini; Dipartimento di Ingegneria dell'Informazione, Università di Padova, Via Gradenigo 6/A, 35131 Padova

Over the past decade, GaN power transistors have emerged as excellent devices for application in power electronics. Thanks to the high breakdown field, the high electron mobility and the wide energy gap of GaN, high temperature and high power transistors can be fabricated, with significant advantages in terms of performance and reliability compared to the silicon counterparts. This tutorial will constitute an excellent opportunity for researchers willing to approach the field of GaN devices, and for scientists/professionals looking for an update in the field of GaN reliability physics. Specific topics that will be covered include properties of GaN and related materials, operation of GaN transistors, dynamic- on resistance and related physics, trapping phenomena in GaN under soft- and hard-switching operation, reliability-limiting mechanisms for GaN transistors. Updates on recent reliability reports will also be presented, to provide a comprehensive overview of the topic.

Tutorial 9
Monday, March 28, 08:30 a.m. – 10:00 a.m. CDT
Venue: Cap Rock I, II & III

08:30 a.m.
TuT9 (Tutorial) - Flash Memory Reliability and Error Mitigation in Modern SSDs, Nikolaos Papandreou, Haralampos Pozidis; IBM

3D NAND flash memory has made inroads into the enterprise storage space and the data center, creating a new tier between fast, volatile main memory and slow, non-volatile hard-disk drives. Moreover, the technological advancements in multiple fronts, e.g., vertical integration, write algorithms, etc., have enabled quad-level cell (QLC) NAND flash which offers further capacity increase and cost-per-bit reduction. These advances make SSD technology attractive for new applications and workloads such as AI and cloud computing. At the same time, however, 3D NAND flash exhibits reliability challenges that affect both the resiliency and performance at the system level, e.g., higher RBER, threshold voltage instabilities, increased read latency, etc. To meet the reliability and endurance requirements of enterprise systems, the NAND flash memory controller needs to accommodate advanced flash management and error-handling algorithms. This tutorial is organized in two parts. The first part will cover the reliability challenges of 3D NAND flash in modern SSDs. We will discuss the reliability challenges of 3D NAND flash with a focus on the device- and system-level aspects. We will review the device reliability issues related to endurance, retention, read disturb, open blocks and other transient effects and discuss the effect of those factors at the system level. The second part will cover various flash management algorithms employed in state-of-the-art NAND flash controllers. Emphasis will be given to error mitigation and media management techniques such as read-voltage calibration, error handling, wear-leveling, health-binning, etc. Finally, a review of modern SSD applications and their challenges will be provided.

Tutorial 10
Monday, March 28, 08:30 a.m. – 10:00 a.m. CDT
Venue: Becker I & II

08:30 a.m.
TuT10 (Tutorial) - Advanced CMOS Technology Challenges for Robust ESD Design, Shih-Hung Chen; imec

Bulk FinFET has been a mainstream CMOS technology in sub-20nm nodes because of improved channel

electrostatic and leakage control. ESD reliability has been investigated in bulk FinFET and is strongly impacted by newly introduced process options in the advanced technology nodes. These process options include self-align multiple patterning lithography, local interconnect (LI) defined contact scheme, and S/D epitaxial growth in different process modules. They can bring significant impacts on ESD failure level, clamping voltage and turn-on efficiency.
Besides of ESD reliability, higher supply voltages (e.g., 1.8V or 3.3V) are still required in external I/O interface circuits and some analog circuits in bulk FinFET technologies. The I/O transistors concerning about latchup (LU) prevention are also influenced by the specific process options in sub-20nm nodes.
Next to the FinFET technology, a gate-all-around (GAA) nanowire (NW) technology is a promising candidate for sub-10nm nodes. This new transistor architecture will also bring impacts on ESD device characteristics. Not only the novel transistor architectures, but new technology scaling concepts have been also proposed, for example, design-technology co-optimization (DTCO) scaling options, and system-technology-co-optimization (STCO). The corresponding influences of these future technologies on ESD reliability will also need to be further evaluated.
In this tutorial, we will look at the influence of the device architectures and the corresponding process options on ESD device characteristics in the FinFET/GAA NW technologies. 3D TCAD simulations bring an in-depth physical understanding of the ESD current conduction and failure mechanism in the ESD protection devices.

Break
Monday, March 28, 10:00 a.m. – 10:30 a.m. CDT

Tutorial 11
Monday, March 28, 10:30 a.m. – 12:00 p.m. CDT
Venue: International I & II

10:30 a.m.
TuT11 (Tutorial) - RF/mmW/5G Reliability, Sriram Kalpat; Qualcomm

RF wireless communication has seen an exponential growth since its introduction in the early 1980s. A new generation is introduced every ten years, currently the fifth generation (5G) is in its deployment phase. 5G frequency bands have moved up from the crowded and fractural LTE bands to higher sub-6 GHz bands and into the millimeter wave (mmWave) spectrum that allows wider bandwidth support. Current advanced CMOS technologies are excellent candidates to meet the low cost and high-volume demand of mmWave technology. CMOS RF mmWave system-on-chip (SOC) solution with integrated switch, LNA, phase shifter, local oscillator, mixer, PA, along with digital control blocks have been achieved at low cost and high-volume manufacturing. Today, 5G mmWave technology is a commercial reality which offers wider signal bandwidths, higher data rate communication and lower latency.
This tutorial provides an overview of RF/mmWave/5G technology and its critical reliability challenges. It reviews the device reliability requirements of the key RF circuit blocks namely the PA, LNA and switch. The tutorial also addresses future challenges to CMOS mmWave scaling and discusses the viable technology options.

Tutorial 12
Monday, March 28, 10:30 a.m. – 12:00 p.m. CDT
Venue: International III & IV

10:30 a.m.
TuT12 (Tutorial) - Effects of Defects in SiC Epilayers on Device Yield and Reliability, Bob Stahlbush; Navy Research Lab

The potential of SiC power devices to deliver better performance than Si power devices has become a commercial reality in the last few years. Compared to Si, SiC has a 3X larger bandgap, a 10X higher breakdown field, and 3X higher thermal conductivity. These advantages provide the potential to design more compact, higher efficiency power electronics systems. A crucial factor that has enabled the commercial viability of SiC

power devices has been the reduction of extended defects within the active volume of SiC devices. In this tutorial, basal plane dislocation (BPDs) and other extended defect that affect device yield, performance and reliability are discussed. The origin of these defects is discussed, as well as their effect on device yield and reliability. Special attention is given to BPDs for two reasons. First, there are multiple mechanisms for creating them, and second, they have the strongest effect on device reliability. Join the tutorial, to learn more about BPDs and the other extended defects: their origin, their adverse effects on devices, and methods to image and count them.

Tutorial 13
Monday, March 28, 10:30 a.m. – 12:00 p.m. CDT
Venue: Cap Rock I, II & III

10:30 a.m.
TuT13 (Tutorial) - Phase Change Memory (PCM) and STT-MRAM, Wanki Kim, Richard G (Ricki) Southwick; IBM

PCM is relatively mature emerging memory technology which shows promise for serving as a Storage Class Memory (SCM) and for use as synaptic elements to build prototype deep neural networks (DNN) for in-memory computing.
STT-MRAM has also emerged as a leading nonvolatile memory currently used as a stand alone chip and as an embedded memory.
This tutorial will give a broad overview of PCM reliability as well as MRAM operation, integration, and performance trade-offs. Particular attention will be given to endurance.

Tutorial 14
Monday, March 28, 10:30 a.m. – 12:00 p.m. CDT
Venue: Becker I & II

10:30 a.m.
TuT14 (Tutorial) - SOC ESD Design and Verification, Hans Kunz; Texas Instruments

While the need for on-chip ESD protection may be well understood, many misunderstandings exist about how that protection is achieved. These misunderstandings often lead to insufficient structure around the on-chip ESD design and verification process—resulting in poor on-chip ESD performance and generating unintended troubleshooting activity and circuit re-design.
This seminar will explore these misunderstandings, and identify key aspects of the ESD design process that must be considered. Further, this seminar will explore the ESD verification process as it reflects the ESD design process. This seminar will also examine the design and verification tools environment and identify unintended restrictions that must be overcome.

Break
Monday, March 28, 12:00 p.m. – 01:00 p.m. CDT

Tutorial 15
Monday, March 28, 01:00 p.m. – 02:30 p.m. CDT
Venue: International I & II

01:00 p.m.
TuT15 (Tutorial) - High-Density Electronic Circuits Made of 2D Materials: Towards their Integration in CMOS Silicon Chips, Mario Lanza; KAUST

Two-dimensional layered materials (2D-LMs) materials have outstandingphysical, chemical and thermal properties that make them attractive for thefabrication of solid-state micro/nano-electronic devices and circuits.

However, synthesizing high-quality 2D-LMs at the wafer scale is difficult, and integratingthem in semiconductor production lines brings associated multiple challenges. Nevertheless, in the past few years substantial progress has been achieved andleading companies like TSMC, Samsung and IMEC have started to work moreintensively on the fabrication of devices using 2D-LMs. In this tutorial, I will discussthe state-of-the-art on micro/nano-electronic devices made (entirely or partially) of 2D-LMs, as well as their integration in CMOS chips. I will present the mostsophisticated prototypes developed so far, with special emphasis on devices thatemploy hexagonal boron nitride, the only 2D-LM with an enough high band gapto be employed as dielectric. I will also discuss the main technological challengesto face in the next years and provide some recommendations on how to solve them.

Tutorial 16
Monday, March 28, 01:00 p.m. – 02:30 p.m. CDT
Venue: International III & IV

01:00 p.m.
TuT16 (Tutorial) - Automotive Use Conditions—Trends & Reliability Challenges, Jyotika Athavale; NVIDIA

Autonomous vehicle architectures are becoming more integrated and increasingly complex to achieve leading-edge functionality. Mitigations to realize reliability performance for these multi-core System-ona-chip (SoC)-based systems can be expensive and challenging. This is especially true when considering the stringent and evolving use-condition requirements for these applications, such as longer mission times and higher utilization rates. Compliance to transient reliability requirements is of paramount importance. Furthermore, when considering soft-error performance, we need to focus on accurately modeling vulnerability factors for transient error-rate modeling based on AI and deep learning workloads. Reliability of highly dense nodes and smaller geometries requires innovative methods and mitigations in process technology, architecture, design and software.

Tutorial 17
Monday, March 28, 01:00 p.m. – 02:30 p.m. CDT
Venue: Cap Rock I, II & III

01:00 p.m.
TuT17 (Tutorial) - Probabilistic Design for Reliability in Electronics and Photonics: Role, Significance, Attributes, Challenges, Ephraim Suhir; Portland State University and ERS Co.

The probabilistic design for reliability (PDfR) concept in electronics and photonics (EP) engineering is based on 1) highly focused and highly cost-effective failure oriented accelerated testing (FOAT), aimed at understanding the physics of the anticipated failures and at quantifying, on the probabilistic basis, the outcome of FOAT conducted for the most vulnerable element(s) of the product of interest considering its most likely applications and the most meaningful combination of possible stressors (stimuli); 2) simple and physically meaningful predictive models (PM), both analytical and computer-aided, such as, e.g., multi-parametric Boltzmann-Arrhenius-Zhurkov (BAZ) equation, aimed at bridging the gap between the FOAT data and the most likely field conditions; and 3) subsequent FOAT data and PM based sensitivity analyses (SA). These analyses just use the methodologies and algorithms developed as by-products at the two previous steps. The PDfR concept proceeds from the recognition that nothing is perfect and that the difference between a highly reliable and an insufficiently reliable product is “merely” in the level of the never-zero probabilities of their failure. If the probability of failure and the corresponding lifetime, evaluated for the anticipated loading conditions and the given time in operation, is not acceptable, SA can be effectively employed to determine what could/should be changed to improve the situation.

Tutorial 18
Monday, March 28, 01:00 p.m. – 02:30 p.m. CDT
Venue: Becker I & II

01:00 p.m.
TuT18 (Tutorial) - Analog ESD Design Integration Challenges, Raj Sankaralingam; Texas Instruments

On-chip analog ESD design integration is highly product specific unlike IO-based approach in digital products. In addition, large number of components in BCD technologies makes it challenging to design for efficient ESD protection due to tradeoffs between ESD vs design performance vs cost. In this seminar, we will discuss pros and cons of various ESD integration methods – manual, topology checker based, and simulation based. We will also discuss some of the challenges with designing for HBM, CDM and system level ESD specifications.

Break (All breaks are in the: International Foyer)
Monday, March 28, 02:30 p.m. – 03:00 p.m. CDT

Reliability Year-in-Review
Monday, March 28, 03:00 p.m. – 05:30 p.m. CDT
Venue: International III & IV

03:00 p.m.
YIR1 (Year-in-Review) - 3D IC Packaging, Kangwook Lee; SK Hynix

TBD

03:50 p.m.
YIR2 (Year-in-Review) - Emerging Memory Reliability (MRAM, RRAM, PCM, Ferroelectrics), Shimeng Yu; Georgia Institute of Technology

We will review the progresses of the reliability characterization of the emerging memories in the past two years. The devices of interests include MRAM, RRAM, PCM and Ferroelectrics.

04:40 p.m.
YIR3 (Year-in-Review) - Reliability and Aging Aware Designs/Circuit Reliability, Evelyn Landman; proteanTecs

Since silicon technologies were first introduced, failure modes were studied, and test procedures standardized to assure reliability in lifetime operation. Mission-critical applications are dominating semiconductor consumption, leading to emerging reliability challenges due to advanced designs and manufacturing technologies and increased performance requirements. This presentation will cover advancements in circuit reliability, including reliability characterization techniques (novel methodologies and EDA), solutions for 3D IC reliability, and novel circuits and methods for more robust reliability.

Tuesday March 29

Welcome & IRPS Introduction
Tuesday, March 29, 08:00 a.m. – 08:35 a.m. CDT
Venue: International III & IV

Keynote 1
Tuesday, March 29, 08:35 a.m. – 09:20 a.m. CDT
Venue: International III & IV

08:35 a.m.
KN1 (Keynote) - Reliability at Scale: Pushing the Boundaries of Reliability and Quality at the Frontiers of Compute, Mohsen Alavi, Intel, United States

Semiconductor scale is accelerating as the aggregation of very large areas of silicon at the component level amplifies continued Moore's law scaling to meet the demand for computational capacity. The increasing dependence on these capabilities to support the world's critical data center infrastructure is also resulting in quality and reliability expectations from hyperscale installations to the 'edge' which are far more demanding than those of specialized 'mission critical' applications a decade ago. These factors present compelling challenges for semiconductor component and system reliability, namely, the need for lower component failure rates and extremely low data error rates against the backdrop of rapid Si area growth, complex heterogeneous integration, and Si-package technology advances. Addressing reliability at this scale requires characterization and modeling of failure, degradation, and error rate phenomenon to the extremes of variation (single-digit effects / trillion transistors), and requires innovations in fault tolerance, component, and circuit resiliency as well as Si-package process technologies. The future of semiconductor reliability lies in advancing the state of the art in all these disciplines, and providing efficient, holistic solutions from component to system level to meet the needs of the rapidly expanding compute ecosystem.

Keynote 2
Tuesday, March 29, 09:20 a.m. – 10:05 a.m. CDT
Venue: International III & IV

09:20 a.m.
Keynote 2 - Silicon Lifecycle Management: Increasing Semiconductor Predictability in an Unpredictable World, Shankar Krishnamoorthy; Synopsys, United States

A new paradigm of silicon insights is emerging between synergistic embedded sensing technologies and big data lifecycle assessment and analytics. Significant value-driven opportunities lie with new concepts for assessing the reliability and resilience of silicon devices, from data gathered during design, manufacture, test and in-field. Silicon data driven analytics are providing new actionable insights which begin to address the challenges posed to large scale silicon designs of unpredictability due to process variability, mission mode workload variability and long-term silicon aging effects. By increasing our awareness we are able to enhance and better predict reliability, positioning us to eventually determine both the success and fate of deployed silicon-based products.

Break
Tuesday, March 29, 10:05 a.m. – 10:25 a.m. CDT

2A – Intro
Tuesday, March 29, 10:25 a.m. – 10:30 a.m. CDT

2A - GD (Gate/MOL Dielectrics)
Tuesday, March 29, 10:30 a.m. – 12:10 p.m. CDT
Venue: International I & II

10:30 a.m.
2A.1 (Invited) - Finding Suitable Gate Insulators for Reliable 2D FETs, Theresia Knobloch, Yury Yu. Illarionov, Tibor Grasser; Institute for Microelectronics

Field-effect transistors (FETs) based on two- dimensional (2D) materials hold the promise to allow for ultimately scaled channel thicknesses of single monolayers. Due to their atomically small thicknesses, the gate control is enhanced while sizable mobilities in the 2D semiconductors are maintained. Thus, in recent years considerable

research efforts have focused on 2D FETs and explored various 2D semiconductors and their properties. However, the key challenge of finding suitable gate insulators for 2D FETs has yet received little attention. In this paper, criteria are formulated for identifying suitable gate insulators for reliable 2D FETs. The criteria are grouped into three main categories, these are scaling requirements, reduction of insulator-related charge traps, and technological requirements for the insulator deposition. In addition, possible candidates for gate insulators for 2D FETs are evaluated with respect to the formulated criteria, and important research questions for future investigations are identified.

10:55 a.m.
2A.2 - A Flexible and Inherently Self-Consistent Methodology for MOL/BEOL/MIMCAP TDDB Applications with Excessive Variability-Induced Degradation, Ernest Y. Wu, IBM Research Division

In this work, we develop a flexible and inherently self-consistent grand methodology to resolve the excessive variability-induced degradation encountered in measurements of time-dependent dielectric breakdown (TDDB). This methodology is based on the underlying percolation principle in terms of thickness-dependence of characteristic breakdown time (T63) and Weibull slope (β). Starting from an ideal β thickness-vs-dependence, this methodology involves the use of an iteration procedure for the adjustment of the β-vs-thickness relation for the optimal coefficients to obtain the simultaneous agreement with multiple sets of experimental data. Moreover, we show different governing statistical distributions, (normal or Weibull), and their bimodality for dielectric thickness variation, can also play a great role in affecting final TBD failure distributions. Due to the rigor of our methodology, it can be used for both reliability assessment and lifetime projection.

11:20 a.m.
2A.3 - Bias Temperature Instability (BTI) of High-Voltage Devices for Memory Periphery, Joao Bastos, Barry O'Sullivan, Jacopo Franco, Stanislav Tyaginov, Brecht Truijen. Adrian Chasin, Robin Degraeve, Ben Kaczer, Romain Ritzenthaler, Elena Capogreco, Eugenio Dentoni Litta, Alessio Spessot; imec, Yusuke Higashi; kioxia, Younggwang Yoon; SK Hynix, Vladimir Machkaoutsan, Pierre Fazan; micron, Naoto Horiguchiimec

This paper reports BTI trends in high-voltage transistors for memory periphery devices with SiO**2**/Poly-Si and High-K/Metal gate stacks. For PBTI, we present an extension to the typical power law kinetics that is related to the creation of interface states due to hot electrons transported through the gate oxide. This extension enables a good fit of accelerated test data and, thereby, lifetime extrapolation. We then explore EOT and gate stack trends in PBTI. For NBTI, we report gate stack, EOT, and thermal budget trends.

11:45 a.m.
2A.4 - The Relevance of Trapped Charge for Leakage and Random Telegraph Noise Phenomena, Sara Vecchi, Paolo Pavan, Francesco Maria Puglisi; University of Modena and Reggio Emilia

The current understanding of key reliability phenomena such as leakage and Random Telegraph Noise (RTN) is still incomplete. Models exist that explain simple cases (2-level RTN), yet experimental reports showed the occurrence of complex cases (e.g., coupled RTN, anomalous and temporary RTN) that deserve deeper investigation. In this paper, we focus on the often overlooked role of trapped charge in the electrostatic coupling among defects, entailing a multi-body problem, and on the related effects on leakage and RTN. The electric field in the dielectric is found to be usually dominated by the trapped charge rather than by the applied voltage, defying common beliefs and elegantly explaining some of the aforesaid complex scenarios. We demonstrate that such defects interactions are responsible for a strong modulation of the capture and emission time constants over time. Moreover, we highlight how defects capture/emission source/destination can change with the local field and therefore with the applied voltage, which gives rise to non-monotonic trends in τ_c/τ_e vs. applied voltage plot. This last point reveals that the classical formula adopted for the estimation of the defects vertical position within the dielectric is oversimplified and may lead to significant errors. The results of this study advance the understanding of leakage and RTN, and can be useful for the design of applications such as low-power Physical Unclonable Functions and True Random Number Generators.

2A – Authors' Corner
Tuesday, March 29, 12:10 p.m. – 12:30 p.m. CDT

2B – Intro
Tuesday, March 29, 10:25 a.m. – 10:30 a.m. CDT

2B - GaN (GaN Power Device)
Tuesday, March 29, 10:30 a.m. – 12:10 p.m. CDT
Venue: International III & IV

10:30 a.m.
2B.1 - Vertical GaN Fin JFET: A Power Device with Short Circuit Robustness at Avalanche Breakdown Voltage, R. Zhang, J. Liu, Q. Li; Virginia Polytechnic Institute and State University, S. Pidaparthi, A. Edwards, C. Drowley; NexGen Power Systems Inc, Santa Clara, Y. Zhang, Virginia Polytechnic Institute and State University

GaN high-electron-mobility transistors (HEMTs) are known to have no avalanche capability and insufficient short- circuit robustness. Recently, breakthrough avalanche and short- circuit capabilities have been experimentally demonstrated in a vertical GaN fin-channel junction-gate field-effect transistor (Fin-JFET), which shows a good promise for using GaN devices in automotive powertrains and electric grids. In particular, GaN Fin-JFETs demonstrated good short-circuit capability at avalanche breakdown voltage (BVAVA), with a failure-to-open- circuit (FTO) signature. This work presents a comprehensive device physics-based study of the GaN Fin-JFET under short- circuit conditions, particularly at a bus voltage close to BV_{AVA}. Mixed-mode electrothermal TCAD simulations were performed to understand the carrier dynamics, electric field distributions, and temperature profiles in the Fin-JFET under short-circuit and avalanche conditions. The results provide important physical references to understand the unique robustness of the vertical GaN Fin-JFET under the concurrence of short-circuit and avalanche as well as its desirable FTO signature.

10:55 a.m.
2B.2 - Study of Avalanche Behavior in 3 kV GaN Vertical P-N Diode under UIS Stress for Edge-termination Optimization, Bhawani Shankar, Zhengliang Bian, Ke Zeng, Chuanzhe Meng, Rafael Perez Martinez, Srabanti Chowdhury; Electrical Engineering, Stanford University, Brendan Gunning, Jack Flicker, Andrew Binder, Jeramy Ray Dickerson, Robert Kaplar; Sandia National Labs

This work investigates both avalanche behavior and failure mechanism of 3 kV GaN-on-GaN vertical P-N diodes, that were fabricated and later tested under unclamped inductive switching (UIS) stress. The goal of this study is to use the particular avalanche characteristics and the failure mechanism to identify issues with the field termination and then provide feedback to improve the device design. DC breakdown is measured at the different temperatures to confirm the avalanche breakdown. Diode's avalanche robustness is measured on-wafer using a UIS test set-up which was integrated with a wafer chuck and CCD camera. Post failure analysis of the diode is done using SEM and optical microscopy to gain insight into the device failure physics.

11:20 a.m.
2B.3 - Incorporation of a Simple ESD Circuit in a 650V E-Mode GaN HEMT for All-Terminal ESD Protection, Jian-Hsing Lee, Yeh-Jen Huang, Li-Yang Hong, Li-Fan Chen, Yeh-Ning Jou, Shin-Cheng Lin, Walter Wohlmuth; Vanguard International Semiconductor Corp., Chih-Cherng Liao, Ching-Ho Li, Shoa-Chang Huang, Ke-Horng Chen; National Yang Ming Chiao Tung University

In this paper, a simple circuit is incorporated in a 650V E-mode GaN HEMT process technology to protect all terminals against ESD stress from any direction. Even in the worst case, with the gate subjected to negative ESD pulse with respect to grounded drain, the 650V E-mode HEMT can still pass 5kV HBM.

11:45 a.m.
2B.4 (Invited) - Short-Circuit Capability with GaN HEMTs, Davide Bisi, Bill Cruse, Philip Zuk, Primit Parikh, Umesh Mishra; Transphorm, Inc., 75 Castilian Dr., Goleta, Tsutomu Hosoda, Masamichi Kamiyama, Masahito Kanamura; Transphorm Japan Inc., 2-5-15 Shin-Yokohama, Kouhoku-ku

Short-circuit capability with GaN HEMTs is demonstrated thanks to an integrated Short-Circuit Current Limiter (SCCL) and a commercial gate-driver with DESAT protection. The SCCL is applied to GaN HEMTs to achieve a sufficiently long short-circuit withstanding time (SCWT) while retaining competitive on-state resistance. The SCWT is tuned from 0.3 μs to 3 μs (a remarkable 10x increase) with a relatively small penalty in on-resistance, no leakage increase, no threshold voltage degradation and no reliability degradation. The gatedriver has desaturation detection (DESAT) and soft shutdown circuitry to achieve a fast protection response of 800 ns with high noise immunity greater than 100 V/ns. The combination of GaN power devices with SCCL and a commercial gate driver with fast DESAT and high noise immunity allows short-circuit protection and fail-safe operation of GaN power electronics for additional robustness in motor drive applications.

2B – Authors' Corner
Tuesday, March 29, 12:10 p.m. – 12:30 p.m. CDT

2C - Intro
Tuesday, March 29, 10:25 a.m. – 10:30 a.m. CDT

2C - SR (System Electronics Reliability)
Tuesday, March 29, 10:30 a.m. – 12:10 p.m. CDT
Venue: Cap Rock I, II & III

10:30 a.m.
2C.1 - Mission Profile Clustering using a Universal Quantile Criterion, A. Hirler, U. Abelein; Infineon Technologies AG, Am Campeon 1-15, 85579 Neubiberg, M. Büttner; Robert Bosch GmbH, Robert-Bosch-Campus 1, 71272 Renningen, R. Fischbach, A. Krinke; TU Dresden, Helmholtzstr. 10, 01069 Dresden, G. Jerke; Robert Bosch GmbH, Tübinger Str. 123, 72762 Reutlingen, S. Simon; CARIAD SE, Berliner Ring 2, Brieffach 1080/2, 38440 Wolfsburg

The current trend in the automotive industry towards increasingly detailed and more granular mission profiles (MPs) is also giving rise to an enormous number of various MPs, distinguishing each individual application and use case imaginable. To keep an overview in the face of this flood of data, to filter out and select the qualification relevant MPs, and to create a suitable and simply designed reliability requirement, a MP clustering approach using a quantile criterion is presented. This generic approach is universally applicable and therefore not limited to the automotive industry.
Based on equivalent test times (ETTs) and acceleration factors (AFs), after determining the quantile criterion, a representative MP can be selected either from an existing best fit MP or an artificially generated MP, obtained by numerical methods. Furthermore, the coverage of these MP requirements by technology reliability capabilities can be evaluated with ease. This approach is a generic concept and can therefore be applied to all well-known and commonly used damage accumulation and failure acceleration models. In the presented automotive case studies, the temperature accelerated Arrhenius model, multidimensional MPs with temperature and voltage acceleration, the temperature cycling Coffin-Manson model as well as a non-linear damage accumulation model are investigated.

10:55 a.m.
2C.2 - System-Level Simulation of Electromigration in a 3 nm CMOS Power Delivery Network: The Effect of Grid Redundancy, Metallization Stack and Standard-Cell Currents, Houman Zahedmanesh, Ivan Ciofi, Odysseas Zografos, Kristof Croes; imec Leuven, Mustafa Badaroglu; Qualcomm

A physics-based system-level electromigration (EM) modelling platform is employed to simulate EM and its

impact on the IR drop from the supply voltage to the standard-cells for a power delivery network design in a 3 nm logic node. The simulated PDN elicited high EM-tolerance. Despite EM voiding in multiple PDN segments, the EM induced IR-drop increase at the standard-cell level stayed below 3.3% without any catastrophic standard-cell failures. Use of ruthenium rails reduced IR-drop penalty of system EM by a factor of ~0.6 compared with copper rails.

11:20 a.m.
2C.3 (Invited) - The Price of Secrecy: How Hiding Internal DRAM Topologies Hurts Rowhammer Defenses, Stefan Saroiu, Alec Wolman, Lucian Cojocar; Microsoft

DRAM vendors today choose to keep the internal topologies of DRAM devices secret. This decision introduces significant practical challenges for designers of memory controllers who wish to provide their own forms of Rowhammer defenses. This paper describes three such challenges and the vulnerabilities, inefficiencies, and overhead they introduce. Defenses implemented at the memory controller could reduce (if not eliminate) these deficiencies should internal DRAM topology be made available.

11:45 a.m.
2C.4 (Invited) - Reliability, Availability, and Serviceability Challenges for Heterogeneous System Design,
Majed Valad Beigi, Vilas Sridharan; Sudhanva Gurumurthi; RAS Architecture, AMD, Inc

The demand for high-performance computation continues to accelerate. To satisfy this increasing demand, modern server and high-performance computing systems are increasingly deploying nodes with greater heterogeneity and integration. Both trends reduce the cost of computation: heterogeneity by increasing absolute performance, and integration by reducing cost per computation. What has not changed, however, are the stringent reliability, availability, and serviceability (RAS) requirements for nodes used in server and high-performance computing systems. A high level of RAS is required to ensure that data centers deploying nodes can correctly perform computations over their expected lifetime.
This paper describes the increased RAS challenges posed by increased heterogeneity and integration. The paper motivates these challenges using data gathered from production systems and presents a case study of the RAS implementation on a highly integrated, heterogeneous node: the AMD EPYC™ and AMD Instinct™ MI250X heterogeneous compute node. Finally, the paper provides a call for standardization to aid in meeting these goals for future data centers.

2C – Authors' Corner
Tuesday, March 29, 12:10 p.m. – 12:30 p.m. CDT

Break
Tuesday, March 29, 12:30 p.m. – 01:30 p.m. CDT

3A – Intro
Tuesday, March 29, 01:30 p.m. – 01:35 p.m. CDT

3A - RT (Reliability Testing)
Tuesday, March 29, 01:35 p.m. – 03:15 p.m. CDT
Venue: International I & II

01:35 p.m.
3A.1 - The Field-Dependence Endurance Model and its Mutual Effect in Hf-Based Ferroelectrics, Y. K. Chang, P. J. Liao, S.H. Yeong, Y.-M. Lin, J.H. Lee, W. Tsai, P. C. McIntyre, C.T. Lin; Taiwan Semiconductor Manufacturing Company, Ltd., Hsinchu, Z. Yu, W. Tsai, P. C. McIntyre; Stanford University

A comprehensive study of electric field (E-field) dependent endurance on Hf-based ferroelectric (FE) fatigue and

breakdown mechanism is presented in this study. Under low E-field, reducing E-field worsens FE fatigue and constrains endurance but with no SILC increase as the result of the domain pinning. While under the high E-field stress, endurance is dominated by the field accelerated breakdown due to the increase of oxygen vacancy generation. By utilizing these distinct FE fatigue characteristics under different bias, the recoverable fatigue and prolonged cycle-to-breakdown is observed through a promising high frequency mixed-signal E-field operation.

02:00 p.m.
3A.2 - Ultra-Fast CV Methods (< 10µs) for Dits Spectroscopy and BTI Reliability Characterization using MOS Capacitors, T. Mota Frutuoso, X. Garros, J. Lugo-Alvarez, R. K. Kammeugne, L. D. M. Zouknak, A. Viey, W. Vandendeale, F. Gaillard; Univ. Grenoble Alpes, CEA, Leti, P. Ferrari; Univ. Grenoble Alpes, Grenoble INP, RFIC-Lab

Two Ultra-Fast capacitance characterization methods based on the displacement current measure are explored for MOS capacitance devices. The first method measure the variation of charge obtained from several 100ns short pulses while the second uses a (1 to 5µs/V) continuous ramp to perform the capacitance measurement. Different applications are investigated for each method depending on measurement time and precision. The short pulsed method is used to perform a CV trap spectroscopy. Thanks to distinctive charging and discharging phases we are able to separately extract the capture and emission behavior of interface traps. We demonstrate that BTI characterization can be performed on simple MOScap using CV measurements based on IV ramp as in MOSFET devices. Furthermore, both methods can be combined in oxides presenting a high hysteresis behavior, to separately characterize low frequency oxide trapping from high frequency interface state trapping.

02:25 p.m.
3A.3 - GHz C-V Characterization Methodology and its Application for understanding Polarization Behaviors in High-k Dielectric Films, Yiming Qu, Yang Shen, Mingji Su; College of Information Science & Electronic Engineering, Zhejiang University & International Joint Innovation Center, Zhejiang University, Jiwu Lu; [4]College of Electrical and Information Engineering, Hunan University, Yi Zhao; State Key Laboratory of Silicon Materials, Zhejiang University

In this study, we report an ultra-fast C-V (>4 GHz) measurement methodology for characterizing the high-frequency polarization phenomena in high-k dielectric films (HfO_2 and Al_2O_3). It is confirmed that the methodology based on the displacement current measurement could be applied for GHz CV measurements of high-k dielectric films. Both HfO_2 and Al_2O_3 films show a significant permittivity de-crease under GHz frequencies due to the suppression of ionic polarization. It is the first direct observation of separating ionic and electronic polarization in ultra-thin high-k dielectric films, so far. The phenomena found in this study could be very important for understanding relative physical mechanisms in advanced electron devices, such as ferroelectric and analog devices using high-k dielectric films.

02:50 p.m.
3A.4 (Invited) - Towards the Characterization of Full ID-VG Degradation in Transistors for Future Analog Applications, Pengpeng Ren, Xinfa Zhang, Zhigang Ji; National Key Laboratory of Science and Technology on Micro/Nano Fabrication & Department of Micro/Nano Electronics, School of Electronic Information and Electrical Engineering, Junhua Liu, Runsheng Wang, Ru Huang; National Key Laboratory of Science and Technology on Micro/Nano Fabrication & Institute of Microelectronics

Assessment of transistor degradation in analog circuits during aging effect is challenging due to the wide spread of operating points. This paper presents our proposed characterization approaches of full I_d-V_g degradation for large and nanoscale devices respectively. Threshold voltage shift and mobility degradation in large devices can be extracted simultaneously with fast measurement speed (t_m=3µs). Based on this, full I_d-V_g degradation can be assessed intuitively. Impacts of individual defects on full I_d-V_g degradation in nanoscale devices are characterized with the proposed approach with high resolution. Thus this paper provides a helpful solution to the characterization of device degradation in analog circuits.

3A - Authors' Corner
Tuesday, March 29, 03:15 p.m. – 03:35 p.m. CDT

3B – Intro
Tuesday, March 29, 01:30 p.m. – 01:35 p.m. CDT

3B - WB (Wide-Bandgap Semiconductors (SiC)
Tuesday, March 29, 01:35 p.m. – 03:15 p.m. CDT
Venue: International III & IV

01:35 p.m.
3B.1 - Optical Emission Correlated to Bias Temperature Instability in SiC MOSFETs, Maximilian W. Feil; Institute for Microelectronics & Infineon Technologies AG, Hans Reisinger, André Kabakow, Wolfgang Gustin; Infineon Technologies AG, 85579 Neubiberg, Thomas Aichinger; Infineon Technologies Austria AG, Tibor Grasser; Institute for Microelectronics

Bias Temperature Instability refers to the widely known shift of the threshold voltage of metal-oxide-semiconductor field-effect transistors upon changes of gate bias and is typically measured at room temperature or above. The shift of the threshold voltage is caused by trapping/detrapping of charges in pre-existing defects located close to the semiconductor- insulator interface as well as the generation of new defects. Particularly silicon carbide transistors show a pronounced short- term trapping/detrapping behavior, which leads to threshold voltage variations already well below the microsecond time frame after gate bias changes. The physics of involved charge transfer reactions has been accurately described by non-radiative multiphonon transitions. We present evidence that in SiC devices radiative charge transitions are also present in a Bias Temperature Instability experiment, once the transistor is switched between accumulation and inversion or vice versa. Furthermore, we present a field-effect based pump-probe measurement that allows us to correlate the number of emitted photons after microsecond gate pulses to the threshold voltage recovery.

02:00 p.m.
3B.2 - Investigation of Reliability of NO Nitrided SiC(1-100) MOS Devices, Takato Nakanuma, Asato Suzuki, Yu Iwakata, Takuma Kobayashi, Takuji Hosoi, Takayoshi Shimura, Heiji Watanabe; Graduate School of Engineering, Osaka University, Mitsuru Sometani, Mitsuo Okamoto; National Institute of Advanced Industrial Science and Technology

We systematically investigated the interface properties and reliability of NO nitrided SiC(1100) m-face MOS devices. Although nitridation at 1250°C improved the capacitance-voltage characteristics (i.e., flat-band voltage (V_{fb}) shift and hysteresis), the nitridation reduced the onset field of the *FOWLER-NORDHEIM* current by about 1 $MVcm^{-1}$, causing a higher oxide leakage. Furthermore, the nitrided samples exhibited pronounced V_{fb} shifts in response to both electron and hole injection under a high stress field condition (oxide field: ± 7-8 $MVcm^{-1}$). In addition, when the bias stress condition was chosen on the basis of leakage current density instead of the oxide field, the V_{fb} shifts became similar for samples with different nitridation durations. This indicates that the observed V_{fb} shift is mainly caused by the carrier trapping into pre-existing traps. Our results clearly indicate the drawbacks of nitridation for m-face MOS devices in terms of oxide leakage and V_{fb} instability.

02:25 p.m.
3B.3 - SiO2/4H-SiC Interfacial Chemistry as Origin of the Threshold Voltage Instability in Power MOSFETs, P. Fiorenza, C. Bongiorno, F. Giannazzo, F. Roccaforte; CNR-IMM, Strada VIII n. 5 - Zona Industrale, M. Saggio; STMicroelectronics, A. Messina; CNR-IMM, Strada VIII n. 5 - Zona Industrale & STMicroelectronics

Threshold voltage instability in 4H-SiC MOSFETs was investigated by means of combined cyclic gate bias stress measurements and single gate bias point measurements. This allowed to separate the contributions of interface states (Nit) and near interface oxide traps (NIOTs) in the nitridated deposited gate oxides. Nanoscale chemical

analyses by electron energy loss spectroscopy allowed to correlate these trapping states to the presence of a sub-stoichiometric silicon oxide (~1 nm) and carbon-related defects (<1 nm) on different SiO2/4H-SiC interfaces In particular, the sub-stoichiometric silicon oxide was correlated to the interface states and the carbon-related defects have been correlated to the NIOTs.

02:50 p.m.
3B.4 - Bias Temperature Instability on SiC n- and p-Channel MOSFETs for High Temperature CMOS Applications, Emran K Ashik, Veena Misra, Bongmook Lee; North Carolina State University, Sundar B Isukapati, Woongje Sung, Adam J Morgan, State University of New York Polytechnic Institute, Hua Zhang, Tianshi Liu, Utsav Gupta, Ayman Fayed, Anant K. Agarwal; Ohio State University

The circuit functionalities of Complementary Metal-Oxide-Semiconductor (CMOS) devices on 4H-SiC for digital and analog circuit applications beyond 200°C have been extensively studied, however, the reliability of the devices on SiC needs to be demonstrated due to the traps at/near the dielectric interface. In this report, the reliability of n- and p- Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) has been studied on three different gate oxide conditions - thick thermally grown, ultrathin thermal + thick CVD oxide and ultrathin thermal + thin CVD oxide in terms of their bias temperature instability (BTI) measurement. The MOSFETs were stressed at various constant bias voltages at 150°C and up to 105s. The threshold voltage shift due to positive bias on n-MOSFET is <0.5V after 105s at +25Vwhile p-MOSFET shows a larger shift of -1.9V shift after 105s at -25V and 150 C for ultrathin + thick CVD oxide. The report also establishes improvement in reliability of p-MOSFETs with ultrathin + CVD oxides over thermally grown oxides.

3B - Authors' Corner
Tuesday, March 29, 03:15 p.m. – 03:35 p.m. CDT

3C – Intro
Tuesday, March 29, 01:30 p.m. – 01:35 p.m. CDT

3C - NC (Neuromorphic Computing Reliability)
Tuesday, March 29, 01:35 p.m. – 03:15 p.m. CDT
Venue: Cap Rock I, II & III

01:35 p.m.
3C.1 (Invited) - Sparse and Robust RRAM-based Efficient In-memory Computing for DNN Inference, Jian Meng, Injune Yeo, Li Yang, Deliang Fan, Jae-sun Seo; Arizona State University, Shimeng Yu; Georgia Institute of Technology, Wonbo Shim; Georgia Institute of Technology & Seoul National University of Science and Technology

Resistive random-access memory (RRAM)-based in-memory computing (IMC) recently became a promising paradigm for efficient deep neural network acceleration. The multi-bit RRAM arrays provide dense storage and high throughput, whereas the physical non-ideality of the RRAM devices impairs the retention characteristics of the resistive cells, leading to accuracy degradation. On the algorithm side, various hardware-aware compression algorithms have been proposed to accelerate the computation of deep neural networks (DNNs) computation. However, most recent works individually consider the "model compression" and "hardware robustness". The impact of the RRAM non-ideality for the sparse model is still under- explored. In this work, we present a novel temperature-resilient RRAM-based IMC scheme for reliable DNN inference hardware. Based on the measurement from a 90nm RRAM prototype chip, we first explore the robustness of the sparse model under the different operating temperatures (25° C to 85° C). On top of that, we propose a novel robustness-aware pruning algorithm, then further enhance the model robustness with a novel sparsity-aware noise-injected fine-tuning. The proposed scheme achieves >92% CIFAR-10 inference accuracy after one-day operation, which is >37% higher than the state-of-art method.

02:00 p.m.
3C.2 - Mitigating Read-Program Variation and IR Drop by Circuit Architecture in RRAM-Based Neural Network Accelerators, Nicola Lepri, Artem Glukhov, Daniele Ielmini; Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano and IU.NET

In-memory computing (IMC) with memory arrays allows reducing the time and energy consumption for matrix vector multiplication (MVM) for artificial neural networks (ANN) inference. However, the IMC accuracy is affected by nonidealities, such as program/read variations of device conductance and the parasitic voltage (IR) drop along the wires, whose impact quickly increases when increasing the array size. This work presents new IMC circuit architectures for mitigating both variations and IR drop at the same time. The new schemes allow for improving the accuracy of an ANN from 72.7% to 94.9%, compared to a software accuracy of 96.9%, at the expense of an increase of the memory array area.

02:25 p.m.
3C.3 - Statistical Model of Program/Verify Algorithms in Resistive-Switching Memories for In-Memory Neural Network Accelerators, Artem Glukhov, Nicola Lepri, Daniele Ielmini; Dipartimento di Elettronica, Informazione e Bioingegneria (DEIB), Politecnico di Milano and IU.NET, Valerio Milo; Applied Materials Italia Srl, Andrea Baroni, Eduardo Pérez; IHP-Leibniz-Institut für innovative Mikroelektronik, Cristian Zambelli, Piero Olivo; Dipartimento di Ingegneria, Università degli Studi di Ferrara, Christian Wenger; IHP-Leibniz-Institut für innovative Mikroelektronik & BTU Cottbus-Senftenberg

Resistive-switching random access memory (RRAM) is a promising technology for in-memory computing (IMC) to accelerate training and inference of deep neural networks (DNNs). This work presents the first physics-based statistical model describing (i) multilevel RRAM device program/verify (PV) algorithms by controlled set transition, (ii) the stochastic cycle-to-cycle (C2C) and device-to-device (D2D) variations within the array, and (iii) the impact of such imprecisions on the accuracy of DNN accelerators. The model can handle the full chain from RRAM materials/device parameters to the DNN performance, thus providing a valuable tool for device/circuit codesign of hardware DNN accelerators.

02:50 p.m.
3C.4 (Invited) - Reliability of Non-Volatile Memory Devices for Neuromorphic Applications: A Modeling Perspective, Andrea Padovani, Milan Pesic, Federico Nardi, Valerio Milo, Luca Larcher; Applied Materials Via Meuccio Ruini 74/L, Mondol Anik Kumar, Md Zunaid Baten; Bangladesh University of Engineering and Technology (BUET)

The advent of Artificial Intelligence (AI) and big data era brought an unprecedented (and ever growing) need for fast and energy efficient computation that cannot be obtained with the classical von Neumann computing architecture. This paved the way to new technologies that try to mimic the human brain to leverage its energy efficient and distributed computing. Non-volatile memory technologies seem to be the ideal solution for the hardware implementation of artificial neurons and synapses of Neural Network (NN) architectures and have been extensively investigated in the last years. However, they often suffer from limited linearity and symmetry, poor retention, and high variability, thus requiring significant advancements for their mass adoption in NNs. One of the cornerstones on which the required efforts must be based is certainly represented by device simulations, which can be effectively used to achieve a full understanding of the physics governing the device, which in turn is a pre-requisite for their design, optimization and successful exploitation in neuromorphic applications. In this scenario, we focus on Transition Metal Oxide (TMO)-based RRAM, Ferroelectric Tunnel Junctions (FTJ) and 3D-NAND Charge Trap devices and use simulations to address key issues related to neuromorphic operation (linearity and asymmetry) and reliability (variability and retention).

3C - Authors' Corner
Tuesday, March 29, 03:15 p.m. – 03:35 p.m. CDT

4A – Intro
Tuesday, March 29, 03:35 p.m. – 03:40 p.m. CDT

4A - EM (Emerging Memory)
Tuesday, March 29, 03:40 p.m. – 05:45 p.m. CDT
Venue: International I & II

03:40 p.m.
4A.1 - Electron-Assisted Switching in FeFETs: MW Dynamics – Retention - Trapping Mechanisms and Correlation, Milan Pesic, Bastien Beltrando, Andrea Padovani, Toshihiko Miyashita, Nam-Sung Kim, Luca Larcher; Applied Materials Inc.

We investigate the impact of charge-trapping on ferroelectric (FE) switching and its influence on memory window (MW) and retention of FeFET. Fabricated FinFETs with ferroelectric gate stack were used to study defects properties (within HZO), trapping/FE-switching interplay, and dynamics. Starting from the electronic-assisted nucleation of FE domains, we investigated the interface charging and degradation, as well as their impact on the polarization compensation, MW and stabilization of the retention. Finally, a balance between those competing processes was analyzed and a retention model of FeFET (capturing behavior over device's lifetime) was developed.

04:05 p.m.
4A.2 - MTJ Degradation in SOT-MRAM by Self-Heating-Induced Diffusion, Simon Van Beek, Kaiming Cai, Siddharth Rao, Ganesh Jayakumar, Sebastien Couet, Nico Jossart, Adrian Chasin, Gouri Sankar Kar; imec

In SOT-MRAM, the writing path is decoupled from the reading path and therefore considered robust against MgO breakdown in the MTJ. At operation, high current densities flow through the thin metallic SOT layer underneath the MTJ. We find that the SOT track is robust against electromigration, but we observe failure of the MTJ. A thorough chemical analysis indicates the activation of diffusion mechanisms that degrade the free layer and MgO tunnel barrier.

04:30 p.m.
4A.3 - Investigation of First Fire Effect on VTH Stability and Endurance in GeCTe Selector, P. C. Chang, P. J. Liao, D. W. Heh, C. Lee, D. H. Hou, E. Ambrosi, C. H. Wu, H. Y. Lee, J. H. Lee, X. Y. Bao; Taiwan Semiconductor Manufacturing Company

Ovonic Threshold Switching Selector faces challenges of V_{th} stability in intensive applications due to relaxation and the degradation upon endurance cycling. This work investigates the first fire (FF) voltage effects and mechanisms related to the switching characteristics on GeCTe-based selectors. Higher V_{th} stability and more uniform I_{off}-VTH control during endurance cycling were achieved by higher FF design. A power-law model with strong correlation between endurance and pulse-energy was also demonstrated in this study.

04:55 p.m.
4A.4 - Modelling Ultra-Fast Threshold Voltage Instabilities in Hf-Based Ferroelectrics, B.J. O'Sullivan, B. Truijen, V. Putcha, A. Grill, A Chasin, G. Van Den Bosch, B. Kaczer; imec Leuven, M.N.K. Alam, J. Van Houdt; KU Leuven

Temperature dependence of charge capture and emission in HfO_2 and ferroelectric doped HfO_2 are examined over a wide temperature range. Sizeable threshold voltage (V_{th}) instabilities are observed under cryogenic conditions, contrary to expectation of Arrhenius-based defect freeze-out. The observed data is modelled with ultra-fast defect levels, located close to the silicon channel. The impact of these traps at room temperature on ferroelectric devices is significant: capture and emission times lie in the range applied for ferroelectric device operation, and can explain the read-after-write delay incorporated in Si-based ferro (FE-)FET operation.

4A - Authors' Corner
Tuesday, March 29, 05:45 p.m. – 06:05 p.m. CDT

4B – Intro
Tuesday, March 29, 03:35 p.m. – 03:40 p.m. CDT

4B - RF (RF/mmW/5G)
Tuesday, March 29, 03:40 p.m. – 05:45 p.m. CDT
Venue: International III & IV

03:40 p.m.
4B.1 (Invited) - Reliability of CMOS-SOI Power Amplifiers for Millimeter-Wave 5G: The Case for pMOS, Peter Asbeck; Dept. of Electrical and Computer Engineering, Sravya Alluri; Qualcomm Institute, University of California, Narek Rostomyan; IQ-Analog, Inc., Jefy A. Jayamon; Qualcomm, Inc.

Output power and efficiency of CMOS-SOI millimeter-wave power amplifiers strongly depend on transistor reliability considerations. In comparison to nMOS, pMOS has potential reliability advantages due to 1) higher energy barrier to the gate dielectric from the valence band than from the conduction band; 2) lower impact ionization rate for holes than for electrons at a given electric field; 3) lower gate-induced drain leakage channel and parasitic bipolar transistor gain in partially depleted pFETs. As a result, voltage-handling limits due to hot carrier injection and time-dependent dielectric breakdown are relaxed. With power supply voltage of -2.4V for a 2-stack pMOS 27GHz power amplifier IC, saturated output power of 20dBm and power-added efficiency of 52% are demonstrated, record values for CMOS-based 2-stack unit amplifiers. Short-term accelerated reliability tests at power supply voltage of -2.8V show unchanged characteristics after 18 hours at 19 dBm output power, indicating promising reliability. Analysis to extrapolate reliability for 5G modulation is discussed.

04:05 p.m.
4B.2 - Comprehensive Analysis of RF Hot-Carrier Reliability Sensitivity and Design Explorations for 28GHz Power Amplifier Applications, J. Hai; STMicroelectronics & CEA-LETI, Université Grenoble Alpes & RFIC-Lab, Univ. Grenoble Alpes, F. Cacho, J. Forest, V. Knopik; STMicroelectronics, A. Divay, X. Garros; CEA-LETI, Université Grenoble Alpes, E. Lauga-Larroze, J.-D. Arnould, RFIC-Lab, Univ. Grenoble Alpes

Design of reliable and high-performance radiofrequency (RF) power amplifiers (PA) in CMOS technologies is becoming more challenging due to the increasing reliability issues as we approach the scaling limit. To provide insight on hot-carrier injection (HCI) degradation at RF frequencies, this paper presents a comprehensive analysis to study HCI degradation at 28GHz with different PA architectures based on their mission profile via quasi-static approximations. Sensitivity analysis on power amplifier RF performance is also discussed to offer a better understanding on the importance of accurate device and aging behavior modeling.

04:30 p.m.
4B.3 - RF Reliability of CMOS-Based Power Amplifier Cell for 5G mmWave Applications, Aarti Rathi, Abhisek Dixit; Indian Institute of Technology Delhi, P. Srinivasan, Oscar H. Gonzalez, Fernando Guarin; GLOBALFOUNDRIES Inc.

RF reliability of 40-nm PDSOI nFET power amplifier (PA) cell at 26.5GHz is investigated. DC and RF stresses are applied in conducting and non-conducting hot carrier stress modes to study the PA cell RF and DC degradation behavior. The relationship between DC and large-signal RF performance under various RF stress conditions is investigated using DC and RF metrics. The degradation rate depends on RF power and terminal voltages, where ~8X lower degradation is observed at low VGS. During RF stress, the DC performance degradation rate is higher in the linear operating region than the saturation region. The impact of RF stress is amplified in the presence of DC stress, accelerating the degradation of PA cells. For different VGS under RF stress conditions, the lifetime of the PA cell is calculated and compared.

04:55 p.m.
4B.4 - 22FDX™ 5G 28GHz 20dBm Power Amplifier Constant Load and VSWR Accelerated Aging Reliability, G. Bossu, S. Evseev, W. Arfaoui, D. Lipp, M. Siddabathula; GlobalFoundries Dresden, S. Syed, J.A.S. Jerome; Globalfoundries US Inc.

Power Amplifier (PA) is a key component for embedded RF/mmWave on advanced CMOS technologies on the way to replace the III/V technologies. PA reliability has been a long-standing blocker for those applications. In this paper, a novel methodology is introduced based on an automated waveform analysis tool. Simulation aging results are compared with experimental silicon validation stress for a 28GHz high gain RF Power Amplifier (PA) and confirmed. Waveform analysis tool enables a deeper understanding of both continuous waveform (CW) with constant load and ruggedness test, as well as a new perspective about RF/mmWave circuit aging.

05:20 p.m.
4B.5 - Excellent RF Product HTOL Reliability of 5G mmWave Beamformer Chip Fabricated using GF 45RFSOI Technologies, P. Srinivasan, F. Guarin; Quality and Reliability, GLOBALFOUNDRIES, Enkhbayasgalan Gantsog, H. Krishnaswamy, A. Natarajan; Mixcomm-Sivers Semiconductors

RF High Temperature Operating Life (HTOL) of a 5G mmWave beamformer chip is evaluated at 28GHz under worst case operating life conditions. Each packaged chip with 8 channel Power Amplifier used for generating omnidirectional beam was evaluated for >= 120hrs at 0.1%CCDF under accelerated P_{sat} RF stress at T_j ~ 85C. Excellent initial RF metrics were observed for all ~24 samples measured. Overall Pout and gain degrade by <0.5dB while DC current degrades <10% meeting the 10yr product life criteria demonstrating excellent RF HTOL processed using GF 45RFSOI technology. Excellent aging model to hardware correlation was also observed confirming the validity of the models at mmWave frequencies.

4B - Authors' Corner
Tuesday, March 29, 05:45 p.m. – 06:05 p.m. CDT

4C – Intro
Tuesday, March 29, 03:35 p.m. – 03:40 p.m. CDT

4C - PK (Packaging and 2.5/3D Assembly)
Tuesday, March 29, 03:40 p.m. – 05:45 p.m. CDT
Venue: Cap Rock I, II & III

03:40 p.m.
4C.1 (Invited) - Thermal Challenges of 2.5D/3D Packages in High Performance Computing Devices, Kathy Yan; TSMC

With HPC devices continue to scale up for higher power and higher power density, thermal dissipation management for IC packages are becoming an important issue. This paper presents the thermal solution evolution at package level and system level, that drives towards more advanced package TIM1 solution and liquid or immersion cooling solution. Thermal-aware device floorplan, package thermal solution and advanced system cooling solution are critical to enable HPC application.

04:05 p.m.
4C.2 - Reliability Investigation of W2W Hybrid Bonding Interface: Breakdown Voltage and Leakage Mechanism, Lin Hou; Western Digital, Emmanuel Chery, Kristof Croes, Davide Tierno, Soon Aik Chew; IMEC, Yangyin Chen; Western Digital, Leuven, Peter Rakbin; Western Digital, Milpitas, Eric Beyne; IMEC

The electrical reliability of 1 μm pitch wafer-to- wafer (W2W) Cu/SiCN hybrid bonding interface is evaluated. Breakdown voltage distributions of the W2W hybrid stack were acquired using the controlled-IV method.

Assuming a power law model, extrapolation towards use conditions confirm a lifetime above 10 years, with a power law exponent above 10 for temperatures under 175 °C. The conduction mechanism along the Cu/SiCN hybrid bonding interface is found to be Poole-Frenkel emission with energy barrier equals 0.95 eV. Mobile copper could only be observed at temperatures above 200 °C and for fields above 1.5 MV/cm, confirming the good robustness against copper drift for this bonding interface.

04:30 p.m.
4C.3 - New Method to Perform TDDB Tests for Hybrid Bonding Interconnects, B. Ayoub; STMicroelectronics & Univ. Grenoble Alpes & IMS Laboratory, University of Bordeaux, S. Moreau; Univ. Grenoble Alpes, S. Lhostis, P. Lamontagne, H. Combeau, J. G. Mattei; STMicroelectronics, H. Frémont; IMS Laboratory, University of Bordeaux

Hybrid Bonding (HB) is progressing as the major solution for 3D integrated-circuit with pitch reduction becoming the key. Reliability needs to be studied with HB pitch reduction for possible evaluation of new failure mechanisms and modes. In this paper, we developed a new methodology to study Time- Dependent Dielectric Breakdown (TDDB) at HB level that accounts wafer-to-wafer (W2W) overlay variations. Application of this method to a 1.44 µm-pitch 3D stacked test vehicle demonstrates its accuracy. TDDB at Cu/SiO**2** HB interface follows the 1/E model at low electric fields for all studied temperature suggesting that the role of Cu in breakdown is negligible. The acceleration parameter and the activation energy dependence on the electric fields are studied. The cuprous oxide layer which may act as a barrier to Cu diffusion previously highlighted at the Cu/SiO_2 HB interface does not exist for Cu/SiN interfaces as evidenced by EELS study. This might explain the difference in the TDDB acceleration models between HB level and BEoL ones.

04:55 p.m.
4C.4 - A Novel Approach for Assessing Impact of Temperature Hot-Spots on Chip-Package Interaction Reliability, R. Aggarwal, E. Kabir, R. Kasim; Logic Technology Development Quality and Reliability, Intel Corporation, L. Jiang; Logic Technology Development, Intel Corporation, S. Patra; Quality and Reliability Test Chips and Data, Intel Corporation, N. Lajo; Reliability Lab Technology Development, Intel Corporation

Aggressive technology scaling coupled with an insatiable need for high-performance microprocessors has led to a significant increase in power dissipation in integrated circuits. This has, in turn, led to an increase of within-die thermal gradients. In this paper, we present a novel approach of assessing the impact of spatial and temporal hotspots on the chip-package interaction (CPI) reliability of microprocessors using an on-die ring oscillator (ROSC) based heater. The ROSC design enables the generation of temperature hotspots with power densities exceeding 3000 W/cm^2, allowing assessment of its impact on CPI reliability. The fast response of the ROSC heater enables high- frequency thermal cycling, which can be used to assess CPI reliability for cycle counts of the order of a few million. This methodology can be used to mimic the thermal cycling behavior of microprocessors under realistic workloads and can be used as a tool to improve confidence in thermo-mechanical reliability.

05:20 p.m.
4C.5 - Impact of TSV on TDDB Performance of Neighboring FinFET with HK/IL Gate Stacking, H. Zheng, Y. S. Sun, J. L. Huang; Team of Design For Reliability, Hisilicon, Shanghai

It is well known device parameters like mobility can be significantly affected by the stress induced by TSV in 3DIC. For the sake of long-term application, the impact of TSV stress on device reliability also requires attention. This study presents detailed characterization and analysis of TDDB performance of FinFET devices placed in the neighborhood of TSV. It is found the TDDB lifetime of the devices stressed under substrate injection mode could be seriously worsened by neighboring TSV, while that of the devices stressed under gate injection mode only shows moderate degradation. It is proposed the defect generation in high-K layer, which controls the TDDB performance under the former stress mode, may be more sensitive to mechanical stress than that nearby IL/Si interface which dominates under the latter mode. It can be ascribed to considerable charge trappings in HK during stress, which could significantly lower the stiffness of Hf-O and thus reduce the energy required for defect generation under the impact of the stress induced by TSV. It also shows the impact of TSV on TDDB has no

considerable orientation dependence. The study suggests careful characterization of the reliability, other than the performance, of the devices nearby TSV with specifically designed test structure, is essential for evaluation of TSV- enabled 3DIC.

4C - Authors' Corner
Tuesday, March 29, 05:45 p.m. – 06:05 p.m. CDT

IRPS 2022 WORKSHOPS

**Workshops available to on-site attendees only*

Tuesday, 29 March

6:05 -7:00 PM

Workshop Reception

Bonnie & Clyde Pavilion

7:00-7:55 PM

WS 1 - Dawn or Dusk of Transistor Reliability Physics

Chaired By: Nuo Xu, TSMC & Muhammad Ashraful Alam, Purdue University

International I & II

WS 2 - Neuromorphic Computing

Chaired By: Gennadi Bersuker, Aerospace Corp

International III & IV

WS 3 – Transient Reliability for Wide Bandgap (GaN and SiC) Power Devices

Chaired By: Sandeep Bahl, Texas Instruments & Daniel Lichtenwalner, Wolfspeed

Cap Rock I, II & III

WS 4 - ESD and Latchup

Chaired By: Hans Kunz, Texas Instruments, Vijay Reddy, Texas Instruments

& Harald Gossner, Intel

Becker I & II

WS 5 - Failure Analysis

Chaired By: Bryan Tracy, Tesla Motors

Cross Timbers I & II

7:55-8:05 PM

Break

8:05-9:00 PM

WS 6 - Gate All Around Devices: Performance Improvement at What Reliability Cost?

Chaired By: Adrian Chasin, imec & Inanc Meric, Intel Corporation

International I & II

WS 7 - Process Integration: Does the antenna ratio definition in the design manual guarantee the required reliability lifetime of your products?

Chaired By: Andreas Martin, Infineon

International III & IV

WS 8 - The Future of Memory – Will Emerging Technologies "*Displace* or *Replace*" Conventional DRAM and NAND?

Chaired By: Barry O'Sullivan (IMEC) & Chris Conner (Intel)

Cap Rock I, II & III

WS 9 - The JESD78F spec revision is released. What has changed and what impact could it have?

Chaired By: Michael Stockinger, NXP

Becker I & II

WS 10 - TDDB: The Most Agreed Upon Disagreement

Chaired By: Zakariae Chbili, Intel

Cross Timbers I & II

Wednesday, March 30

Keynote 3
Wednesday, March 30, 08:00 a.m. – 08:45 a.m. CDT
Venue: International III & IV

08:00 a.m.
KN3 (Keynote) - Transformation of Memory and Storage Hierarchy: Enabling High Performance, Reliable, and Sustainable Compute Applications, Nagasubramaniyan Chandrasekaran; Micron Technology

We live in a world of data-intensive systems and applications, fueled by the integration of AI tools in our daily routines, driving exponential growth in our memory and storage systems capacity. Our memory and storage hierarchy has developed around existing technology, and while there is still significant room for optimization in this space, we see a greater need to introduce new technologies in the future. To meet the evolving demand for higher performance, lower power, improved reliability and cost, the memory hierarchy is seeing an expansion with new memory solutions. At the same time, we are seeing a convergence of storage and memory applications. Significant opportunities are emerging, for high bandwidth and high-capacity memories to improve the bottleneck and performance limitations of traditional DDR memory systems. On the other end of the hierarchy, storage solutions are evolving into high performance storage space while continuing to drive cost scaling. Such new memory and storage solutions require innovation in materials, device, process, packaging, and systems technology. While we continue to grapple with cost, performance, and reliability optimization challenges, we must also find solutions that enable sustainable manufacturing and products. In this keynote, we will present some of the challenges the industry is facing and opportunities ahead to continue to meet the requirements across the applications landscape.

Break
Wednesday, March 30, 08:45 a.m. – 09:05 a.m. CDT

5A – Intro
Wednesday, March 30, 09:05 a.m. – 09:10 a.m. CDT

5A - PI (Process Integration)
Wednesday, March 30, 09:10 a.m. – 10:25 a.m. CDT
Venue: International I & II

09:10 a.m.

5A.1 (Invited) - Plasma Processing Induced Charging Damage (PID) Assessment with Appropriate fWLR Stress Methods Ensuring Expected MOS Reliability and Lifetimes for Automotive Products, Andreas Martin; Corporate Reliability Department, Infineon Technologies AG

A stress and measurement sequence is presented for the detection of plasma induced damage instabilities during process reliability monitoring on product wafers of integrated circuit mass production. The significance of a lifetime estimation from data of antenna test structures is demonstrated with respect to automotive quality requirements in contrary to commonly used approaches in industry. It is shown that a comprehensive approach is necessary starting with appropriate test structures, the PID process qualification and the definition of sophisticated design rules. A short constant current stress as revealing reliability stress for hidden damage fulfills the demands and is discussed in detail including a literature review.

09:35 a.m.

5A.2 - Evaluating Forksheet FET Reliability Concerns by Experimental Comparison with Co-Integrated Nanosheets, E. Bury, A. Chasin, B. Kaczer, J. Franco, R. Ritzenthaler, H. Mertens, P. Weckx, N. Horiguchi, D. Linten; imec, M. Vandemaele; KU Leuven, ESAT, S. Tyaginov; A.F. Ioffe Physical-Technical Institute

A novel forksheet (FSH) FET architecture has been proposed earlier, consisting of vertically stacked n- and p-type sheets at opposing sides of a dielectric wall, particularly beneficial for logic cell track height scaling. In this paper, we evaluate the reliability concerns of FSH FETs by experimental comparison with nanosheets (NSH) FETs co-integrated on a single wafer. We report no supplementary charge trapping phenomena being observed notwithstanding the presence of a SiN wall in the FSH architecture. After accounting for processing imperfections (a high-resistive contact to one of both channels) in the FSH device, we conclude that both bias temperature instabilities (BTI) and hot carrier degradation (HCD) reliability are comparable in FSH and NSH. Joint with theoretical calculations of expected horizontal electric fields and worst-case charge trap densities in the SiN dielectric wall in CMOS implementation, we conclude that introducing the FSH architecture does not constitute additional reliability concerns.

10:00 a.m.

5A.3 - Parasitic Drain Series Resistance Effects on Non-Conducting Hot Carrier Reliability, M. J. Hauser, P. Srinivasan, A. Vallett, R. Krishnasamy, F. Guarin, D. Brochu, V. Pham, B. Min; Technology Reliability and Developement, Globalfoundries US Inc

Two key mechanisms (i) trapping induced *PARASITIC DRAIN SERIES RESISTANCE* (PDSRI) and (ii) interface state generation ΔN_{it} are both identified within non-conducting hot carrier injection (NCHCI). During NCHCI stress, the drain current degradation due to PDSRI is observed at the first time readout as a sudden shift and is followed by conventional (relatively lower) monotonically increasing shift due to interface state generation. The convolution of these two phenomena, complicates the extraction of their unique model parameters and lifetime extrapolation. Characterization methods to isolate each is demonstrated. Their separate dependencies on gate length, drain voltage, and temperature are studied and modeled. Using TCAD simulations, the differences in the damage rate and location due to PDSRI and ΔN_{it} are studied. By understanding the E-field distribution, the charge trapping in the side wall spacer region is found to be the key contributor to PDSRI behavior under NCHCI conditions.

5A - Authors' Corner
Wednesday, March 30, 10:25 a.m. – 10:45 a.m. CDT

5B – Intro
Wednesday, March 30, 09:05 a.m. – 09:10 a.m. CDT

5B - WB (Wide-Bandgap Semiconductors (SiC)

Wednesday, March 30, 09:10 a.m. – 10:25 a.m. CDT
Venue: International III & IV

09:10 a.m.
5B.1 (Invited) - Performance Improvement and Reliability Physics in SiC MOSFETs, T. Kimoto, K. Tachiki, A. Iijima, M. Kaneko; Department of Electronic Science and Engineering, Kyoto University

Significant improvement of channel mobility in SiC MOSFETs with high reliability and deep understanding of bipolar degradation in SiC are presented. By excluding oxidation of SiC while adopting H_2 etching prior to oxide formation and interface nitridation, a low interface state density of 6×10^{10} $cm^{-2}eV^{-1}$ near the conduction band edge was achieved in SiC (0001) MOS structures, which resulted in more than two-fold improvement of channel mobility. A physics-based model for stacking fault expansion upon excess carrier injection is proposed. The critical excess carrier density for stacking fault expansion was estimated to be $(4\text{-}6)\times10^{14}$ cm^{-3} at 300 K. A design guideline of a "recombination-enhancement layer", which prevents hole injection into the underlying substrate, is described.

09:35 a.m.
5B.2 - Analysis and Modeling of Vth Shift in 4H-SiC MOSFETs at Room and Cryogenic-Temperature, F. Masin, C. De Santi, G. Meneghesso, E. Zanoni, M. Meneghini; Department of Information Engineering, University of Padova, A. Stockman, J. Lettens, F. Geenen, P. Moens, onsemi, Westerring 15, B-9700 Oudenaarde

We investigate and model the threshold voltage instabilities of 4H-SiC power MOSFETs at room and cryogenic temperatures, based on wide time range (from μs to ks) PBTI analysis. We show that for T > 200 K a stretched (log-like) de-trapping transient dominates the recovery kinetics, while at lower temperatures (down to 80 K) a fast exponential component is also visible. The charge de-trapping process is modeled as a distribution of traps spread over the midgap, that causes the threshold instability. Results indicate: i) one narrow gaussian energy distribution at the interface, visible at low temperature, which explains the exponential transient behavior for T < 200 K; ii) a broader distribution deeper in energy, that is considered to take into account the logarithmic detrapping kinetics at higher temperatures and the threshold static shift with temperature. The proposed modeling framework can accurately reproduce the experimental results.

10:00 a.m.
5B.3 - Identification of Interface States Responsible for VTH Hysteresis in Packaged SiC MOSFETs, M. Cioni, A. Chini; University of Modena and Reggio Emilia, P. Fiorenza, F. Roccaforte; Consiglio Nazionale delle Ricerche-Istituto per la Microelettronica e Microsistemi, M. Saggio, S. Cascino, V. Vinciguerra, M. Calabretta; STMicroelectronics, A. Messina; Consiglio Nazionale delle Ricerche-Istituto per la Microelettronica e Microsistemi & STMicroelectronics

We investigate the mechanism governing threshold voltage (V_{TH}) hysteresis in packaged SiC MOSFETs. A double-ramp measurement method was employed for this scope, being able to accurately evaluate the time-dependent recovery of the positive V_{TH} shift induced by the sweep-up of the gate voltage. Particularly, we studied the effect of the (i) gate driving voltage (V_{GH}), (ii) recovery time (T_{OFF}) and (iii) temperature (T) on the V_{TH} hysteresis. No appreciable differences were observed among data collected at different V_{GH}, whereas a recovery speed-up was observed at higher *T* values. Temperature dependent measurement of V_{TH} recovery yielded a 0.3 eV activation energy, that has been associated to SiC/SiO_2 interface traps located ~0.3 eV below the SiC conduction band.

5B - Authors' Corner
Wednesday, March 30, 10:25 a.m. – 10:45 a.m. CDT

5C – Intro
Wednesday, March 30, 09:05 a.m. – 09:10 a.m. CDT

5C - EL (ESD and Latchup)
Wednesday, March 30, 09:10 a.m. – 10:25 a.m. CDT
Venue: Cap Rock I, II & III

09:10 a.m.
5C.1 (Invited) - ASM-ESD: A Comprehensive Physics-Based Compact Model for ESD Diodes, S. Khandelwal, D. Bavi; School of Engineering, Macquarie University

This paper presents a new compact model for ESD diodes named Advance SPICE Model for ESD diodes (ASM-ESD). In addition to the current-voltage (I-V) and the capacitance-voltage (C-V) behaviors of the diode under normal operating conditions, ASM-ESD has capabilities to model a plethora of important effects critical for the ESD applications. Model features include the ability to capture the overshoot effects, ambient temperature effects, self-heating effect, post reverse breakdown resistance, parasitic BJT gain, transient behavior of BJT gain and reverse recovery effects in ESD diodes. ASM-ESD model formulations have a physical basis leading to an intuitive extraction flow. Model comparisons with measurements for DC I-V, C-V, and TLP with pulse widths ranging from 200 ns to 1.2 ns are presented. These results demonstrate model accuracy for a full range of ESD event scenarios.

09:35 a.m.
5C.2 - Latchup Vulnerability at the 7-nm FinFET Node, N. J. Pieper, Y. Xiong, A. Feeley, D. R. Ball, B. L. Bhuva; Department of ECE, Vanderbilt University

At the 7-nm bulk FinFET node, latchup effects are seen as limited current increases. In this work, 7-nm node latchup susceptibility is evaluated for terrestrial and space environments as a function of supply voltage, temperature, and particle LET. Holding voltage for latchups is strongly dependent on temperature and was observed to be within 100 mV of nominal supply voltage, showing latchup can be sustained at elevated supply voltages Latchup SE cross-section increases with increasing particle LET, increasing supply voltage, and increasing temperature.

10:00 a.m.
5C.3 - A High Voltage Tolerant Supply Clamp for ESD Protection in a 45-nm SOI Technology, Shudong Huang, Elyse Rosenbaum; Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Srivatsan Parthasarathy, Yuanzhong (Paul) Zhou, Jean-Jacques Hajjar; Analog Devices, Inc., Wilmington

This work presents a high voltage tolerant (HVT) supply clamp for ESD protection, in which the current drive of the clamp during an ESD event is maximized without compromising reliability during normal operation. Similar to prior HVT clamps, ESD current shunting is provided by 3 cascoded NFETs but the novel trigger circuit optimizes the gate bias. The design is implemented in a 45-nm SOI CMOS technology and the clamp devices are sized for a 2-kV HBM protection level. As evidenced by TLP and VFTLP measurements, the new clamp offers 50% reduction of on- resistance and 0.6 V lower turn-on voltage, relative to the prior art.

5C - Authors' Corner
Wednesday, March 30, 10:25 a.m. – 10:45 a.m. CDT

6A – Intro
Wednesday, March 30, 10:45 a.m. – 10:50 a.m. CDT

6A -TX (Transistors)
Wednesday, March 30, 10:50 a.m. – 12:05 p.m. CDT
Venue: International I & II

10:50 a.m.

6A.1 (Invited) - Transistor Reliability Characterization for Advanced DRAM with HK+MG & EUV Process Technology, N-H Lee, S. Lee, S-H Kim, G-J Kim, KW. Lee, YS. Lee, YC. Hwang, HS. Kim, S. Pae; Memory Division, Samsung Electronics, Hwasung

With the growth of high performance computing on many industrial sectors that includes mobile/network and data centers/servers, the need for continued technology scaling and advancements on new process technology have paved ways to manufacture advanced semiconductor products. High-k + Metal gate devices and most recently EUV lithography process have become a key enabler for the 7nm technology nodes and beyond [1]. These technologies are being adopted in the advanced DRAM nodes. DRAM memory uses various devices such as MOSFETs (w/ and w/o HK+MG), cell transistor, cell capacitor, and its reliability has also been considered according to the designed purposes. This paper reviews comprehensive reliability on all types of devices used at each circuit in 15nm DRAM memory. The intrinsic reliability of devices in peripheral regions was guaranteed with systematic wafer-level-reliability evaluation up to product level testing for 1000hrs. The reliability of transistors in core regions was verified using design for reliability, various test structures, and up to an accelerated product level aging test. With the suggested degradation modeling of the capacitor in cell regions, the result on 32GB DIMM field tested for over 1 years shows the best in class reliability results and meets 10yrs of lifetime.

11:15 a.m.
6A.2 - Simulation Comparison of Hot-Carrier Degradation in Nanowire, Nanosheet and Forksheet FETs, Michiel Vandemaele, Guido Groeseneken; ESAT, KU Leuven & imec, Ben Kaczer, Erik Bury, Adrian Chasin, Jacopo Francop, Hans Mertens, Alexander Makarov, Geert Hellings; imec, Stanislav Tyaginov; imec & Russian Academy of Sciences

Forksheet (FS) FETs are a novel transistor architecture consisting of vertically stacked nFET and pFET sheets at opposite sides of a dielectric wall. The wall allows reducing the p- to nFET separation (p-to-n separation), thus enabling further logic cell area scaling without requiring gate length scaling. We report hot-carrier degradation (HCD) simulations of FS FETs and compare this architecture to nanowire (NW) and nanosheet (NS) FETs. HCD is shown to decrease with increasing sheet width in both NS and FS FETs when taking interface state generation into account. Considering that a FS FET can be made wider than an NS FET because of the reduced p-to-n separation, lower HCD for the FS FET is observed. Finally, we make an initial assessment of the impact of oxide defect charging in the FS wall. We confirm decreasing influence of fixed wall charge for increasing sheet widths and estimate that the overall impact of wall charging will stay under control at operating conditions.

11:40 a.m.
6A.3 - Understanding and Modeling Opposite Impacts of Self-Heating on Hot-Carrier Degradation in n- and p-channel Transistors, Stanislav Tyaginov; imec & Russian Academy of Sciences, Alexander Makarov, Al-Moatasem Bellah El-Sayed; Nanolayers, Adrian Chasin, Erik Bury; imec, Markus Jech; Institute for Microelectronics, Technical University of Vienna, Michiel Vandemaele; Department of Electrical Engineering (ESAT), Alexander Grill, An De Keersgieter; imec, Mikhail Vexler; A.F. Ioffe Physical-Technical Institute, Russian Academy of Sciences, Geert Eneman, Ben Kaczer; imec

We extend our framework for hot-carrier degradation (HCD) modeling by covering the impact of self-heating (SH) on HCD. This impact is threefold: (i) perturbation of carrier transport, (ii) acceleration of the thermal contribution to the Si-H bond breakage process, and *(iii)* and shortening vibrational lifetime of the bond resulting in reducing the multiple-carrier mechanism rate. We validate the framework against HCD data acquired on n-channel fin field-effect-transistors (FETs) and p- channel nanowire (NW) FETs under various stress conditions and analyze the importance of each of the aforementioned components of the SH impact on HCD. This analysis shows that in n-channel devices SH depopulates the high energetical fraction of the carrier distribution, while in p-channel transistors SH slightly shifts the carrier energy distribution towards higher energy. Thus, in nFinFETs the impact of SH on the carrier transport and enhancement of the thermal component of bond rupture compensate each other (vibrational lifetime shortening has a weak impact on HCD), thereby leading to slight inhibition of HCD by SH. To the contrary, in pNWFETs these two factors both enhance HCD (while the contribution of the vibrational lifetime dependence on temperature is again small) and thus SH accelerates HCD. Our modeling

framework, therefore, can explain why in n-channel FETs SH slightly inhibits HCD, while in p-channel devices HCD is accelerated by SH.

6A - Authors' Corner
Wednesday, March 30, 12:05 p.m. – 12:25 p.m. CDT

6B – Intro
Wednesday, March 30, 10:45 a.m. – 10:50 a.m. CDT

6B - MR (Memory Reliability)
Wednesday, March 30, 10:50 a.m. – 12:05 p.m. CDT
Venue: International III & IV

10:50 a.m.
6B.1 (Invited) - NanoBridge Technology: Nonvolatile FPGA and Memory Applications, Munehiro Tada, NanoBridge Semiconductor, Inc.

A recent progress of NanoBridge (NB) technology is reviewed in terms of nonvolatile field-programmable gate array (FPGA) and memory (NVM) applications. The NB is a kind type of electrochemical resistive-change device using migration of Cu, in which a thickness of Cu bridge can be controlled by a programming current and an appropriate ON-conductance is programmed for depending on the applications. For a routing switch in the FPGA, two NBs are connected in series and each conductance is tuned to 0.8mS to transfer signals, in which the NBFPGA realizes 78% area and 80% power reductions compared with a conventional SRAM-FPGA. For the NVM application, that is tuned to 0.2mS, which has 150^{o}C 20years retention with 30% degradation of the conductance, which is potentially applicable for automobile/AIoT applications.

11:15 a.m.
6B.2 - New Insight into the Aging Induced Retention Time Degradation of Advanced DRAM Technologies, Yong Liu, Pengpeng Ren, Da Wang, Longda Zhou, Zhigang Ji; National Key Laboratory of Science and Technology on Micro/Nano Fabrication & Department of Micro/Nano Electronics, School of Electronic Information and Electrical Engineering, Junhua Liu, Runsheng Wang, Ru Huang; National Key Laboratory of Science and Technology on Micro/Nano Fabrication & Institute of Microelectronics

In advanced DRAM process node, buried-channel- array transistor (BCAT) in cell-array will generate additional leakage during long-term read/write operations, leading to data retention time reduction. In this work, we designed the accelerated aging test in wafer level and proposed aging leakage model. Based on Monte Carlo simulation, we predict data retention time degradation (especially tail distribution) of high-capacity DRAM under long-term operating conditions. By adding aging leakage model into conventional retention time simulation flow, the data retention time at different operation time can be predicted. It was found that the aging can degraded data retention time in tail distribution around 13% in 10 years. This work is thus helpful to the refresh scheme development considering aging effect.

11:40 a.m.
6B.3 - Extended MTJ TDDB Model, and Improved STT-MRAM Reliability with Reduced Circuit and Process Variabilities, V. B. Naik, J.H. Lim, K. Yamane, J. Kwon, Behin-Aein B., N.L. Chung, S. K, L.Y. Hau, R. Chao, C. Chiang, Y. Huang, L. Pu, Y. Otani, S.H. Jang, N. Balasankaran, W.P. Neo, T. Ling, J.W. Ting, H. Yoon, J. Mueller, B. Pfefferling, O. Kallensee, T. Merbeth, C.S. Seet, J. Wong, Y.S. You, S. Soss, T H. Chan, S.Y. Siah; GLOBALFOUNDRIES Singapore Pte. Ltd.

We present a reliable magnetic tunnel junction (MTJ) TDDB model using 40Mb 22FDX® STT-MRAM at sub-PPM failure rate. This model is based on the precise estimation of voltage across MTJ at bit-cell level derived from compact model and design simulations to cover the product level endurance performance from MTJ

diameter, resistance-area product, and temperature effects. We discuss the implications of pre/post MTJ switching, circuit variations and write pulse on MRAM endurance. By using design-process-test co-optimization, we show robust MRAM product reliability to meet >1M cycles with solder reflows and path towards achieving >E12 cycles for cache applications.

6B - Authors' Corner
Wednesday, March 30, 12:05 p.m. – 12:25 p.m. CDT

6C – Intro
Wednesday, March 30, 10:45 a.m. – 10:50 a.m. CDT

6C - EL (ESD and Latchup)
Wednesday, March 30, 10:50 a.m. – 12:05 p.m. CDT
Venue: Cap Rock I, II & III

10:50 a.m.
6C.1 - Effect of Source & Drain Side Abutting on the Low Current Filamentation in LDMOS-SCR Devices, Monishmurali M, Mayank Shrivastava; Department of ESE, Indian Institute of Science, Nagothu Karmel Kranthi, Gianluca Boselli; Texas Instruments Inc

The concept of abutting source/body and drain/anode junctions is studied in detail in a high voltage LDMOS-SCR with 2D and 3D TCAD simulations. The SCR turn-on and low current filament formation are strongly influenced by the isolation at the anode and cathode side in the LDMOS-SCR. While the anode side isolation impacts the filament-induced failures at low currents, the cathode side isolation has a minor impact. Physical insights are given on the SCR turn-on degradation with abutting and its influence on the filament formation and spreading. The obtained understanding helps to build an ESD robust, self-protected LDMOS-SCRs.

11:15 a.m.
6C.2 - TCAD Investigation of Power-to-Failure Evaluation for Ultrafast Events in BJT-Based ESD Protection Cells, Laura Zunarelli, Susanna Reggiani, Elena Gnani, ARCES and DEI, University of Bologna, Raj Sankaralingam, Mariano Dissegna, Gianluca Boselli; Texas Instruments

The root causes for the anomalous P_f-t_f scaling behavior in the adiabatic regime are identified for a BiCMOS-based ESD protection for the first time. TCAD is used both to understand the turn-on of the integrated architecture with two coupled bipolar transistors under different ESD pulses and to explore the main physical mechanisms leading to the thermal runaway and failure. Simulations clearly show the complex interaction between the conductance modulation and the onset of hot spots in the full volume of the device structure, leading to the identification of critical parameters for the optimization of the proposed ESD cell.

6C - Authors' Corner
Wednesday, March 30, 12:05 p.m. – 12:25 p.m. CDT

Break
Wednesday, March 30, 12:25 p.m. – 01:25 p.m. CDT

7A – Intro
Wednesday, March 30, 01:25 p.m. – 01:30 p.m. CDT

7A - RT (Reliability Testing)
Wednesday, March 30, 01:30 p.m. – 02:45 p.m. CDT
Venue: International I & II

01:30 p.m.
7A.1 - Universal Hot Carrier Degradation Model under DC and AC Stress, Chu Yan, Yaru Ding, Yiming Qu, Liang Zhao; College of Information Science and Electronic Engineering, Zhejiang University & International Joint Innovation Center· Zhejiang University, Yi Zhao; College of Information Science and Electronic Engineering, Zhejiang University & International Joint Innovation Center· Zhejiang University & State Key Laboratory of Silicon Materials· Zhejiang University

In this study, the impact of the self-heating effect (SHE) on the activation energy of hot-carrier injection (HCI) has been studied in n-FinFETs by correcting the channel temperature under different stress patterns. We also experimentally investigated why stress patterns with a shorter pulse width pstress result in a longer device lifetime. In addition to the inevitable SH, time-resolved particle behavior also plays an important role. Based on experimental data and the multiple vibrational excitation theory, a universal model is proposed covering HCI degradation under both DC and AC stress patterns with pstress down to 1 ns.

01:55 p.m.
7A.2 - Comparison of AC and DC BTI in SiC MOSFETs, Amartya K. Ghosh, Osama O. Awadelkarim, Samia Suliman, Xinyu Wang; Dept of Engineering Science and Mechanics, Pennsylvania State University, Jifa Hao; Dept of Engineering Science and Mechanics, Pennsylvania State University & Process and Device Reliability

In this work we compared AC and DC bias temperature instability (BTI) degradations induced by stressing the channel and Junction-FET regions in 4H polytype n-channel Silicon Carbide (SiC) based power MOSFETs. We observed that the degradation caused by AC BTI stress is dependent on the device technology generation unlike the DC BTI stress degradation, which is found to be independent of technology generation. Also, we found that the AC BTI stress causes more permanent damage to the device due to the creation of interface traps and border traps in contrast to DC BTI where only border traps are responsible for the degradation.

02:20 p.m.
7A.3 - Fast Measurement of BTI on 28nm Fully Depleted Silicon-On-Insulator MOSFETs at Cryogenic Temperature Down to 4K, Lauriane Contamin, Mikaël Cassé, Xavier Garros, Fred Gaillard, Maud Vinet; Univ. Grenoble Alpes, Philippe Galy, André Juge, Emmanuel Vincent ; STMicroelectronics Crolles R&D Center, Silvano de Franceschi; Univ. Grenoble Alpes, Tristan Meunier, Univ. Grenoble Alpes

We report preliminary results on bias temperature instabilities (BTI) on 28FDSOI MOS transistors from 300K to 4K with ultra-fast measurements. Common models describe BTI as a temperature-activated effect. Consequently, BTI is expected to be suppressed at cryogenic temperature. However, our measurements show that some BTI degradation remains even at 4K, underlying another degradation mechanism that becomes predominant at low temperature for both PBTI and NBTI. We offer insight into its characteristic temperature and time scales. We study the effect of the back-gate voltage, and show that its use can mitigate BTI degradation. Finally, an anomalous signal is observed in small PMOS devices, which can be caused by a trapping from the gate that is revealed at low temperature.

7A - Authors' Corner
Wednesday, March 30, 02:45 p.m. – 03:05 p.m. CDT

7B – Intro
Wednesday, March 30, 01:25 p.m. – 01:30 p.m. CDT

7B - MR (Memory Reliability)
Wednesday, March 30, 01:30 p.m. – 02:45 p.m. CDT
Venue: International III & IV

01:30 p.m.
7B.1 - Characterization and Modelling of Hot Carrier Degradation in pFETs under Vd>Vg Condition for

sub-20nm DRAM Technologies, Da Wang, Yong Liu, Pengpeng Ren, Longda Zhou, Zhigang Ji; National Key Laboratory of Science and Technology on Micro/Nano Fabrication & Department of Micro/Nano Electronics, School of Electronic Information and Electrical Engineering, Junhua Liu, Runsheng Wang, Ru Huang; National Key Laboratory of Science and Technology on Micro/Nano Fabrication & Institute of Microelectronics, Peking University

pFETs fabricated with the sub-20nm technology are investigated under hot carrier stress conditions of the gate voltage ($|V_g|$) lower than the drain voltage ($|V_d|$). Two types of defects are identified: the interface states generation exhibits the positive charge formation while the electron-traps lead to the negative charge accumulation. The corresponding energy levels and the spatial locations are identified by exploring the defect-induced mobility degradation and the recovery phenomenon. Finally, a defect-based model is proposed for both the threshold voltage shift and the mobility degradation, which allows the full IV to be predicted after aging. Thus the work paves ways for future device/circuit co-optimization in DRAM peripheral circuits.

01:55 p.m.
7B.2 - First Experimental Study of Floating-Body Cell Transient Reliability Characteristics of Both N- and P-Channel Vertical Gate-All-Around Devices with Split-Gate Structures, Cheng-Lin Sung, Sheng-Ting Fan, Hang-Ting Lue, Wei-Chen Chen, Pei-Ying Du, Teng-Hao Yeh, Keh-Chung Wang, Chih-Yuan Lu; Emerging Central Lab. Macronix International Co.

We present results of the first experimental study of floating-body cell (FBC) transient characteristics for both n- and p-channel devices using the vertical split-gate gate-all-around (GAA) structure with channel diameter around 60nm. We applied pulse IV measurements to study our previously developed vertical-channel split-gate Flash memory devices, and observed clear transient behaviors which are verified to be the FBC mechanism. The split-gate structure provides superior merits than 1T structure to help measuring the FBC behaviors because the select gate (SG) can keep stationary bias to avoid capacitive coupling effect to deteriorate the transient charge storage beneath SG. After studying various well doping splits and bias dependence, the maximal V_t shifts we can obtain are only around ~0.38V and 0.32V for n- and p-channel FBC devices, respectively. The retention is only ~80μsec for the n-channel device, but is extended to nearly 10msec for p-channel devices. The FBC V_t shifts and retention degrades significantly at high-temperature (up to 125°C) measurements. 3D TCAD model was well established to explain the FBC characteristics of the vertical split-gate GAA structure, and it predicted that the FBC transient V_t shift window would vanish when the GAA diameter reduced below 40nm, which became fully-depleted floating-body device. This work suggests challenges to pursue FBC as a DRAM replacer, and new innovations are needed for this path. Meanwhile, for ordinary Flash memory or LOGIC operations using GAA devices, the aggressive scaled GAA diameter and suitable low-voltage operations would not suffer trouble in such transient FBC effects.

7B - Authors' Corner
Wednesday, March 30, 02:45 p.m. – 03:05 p.m. CDT

7C – Intro
Wednesday, March 30, 01:25 p.m. – 01:30 p.m. CDT

7C - SE (Soft Errors)
Wednesday, March 30, 01:30 p.m. – 02:45 p.m. CDT
Venue: Cap Rock I, II & III

01:30 p.m.
7C.1 (Invited) - Recent Advances and Trends on Automotive Safety, Riccardo Mariani, Karl Greb; NVIDIA

This paper provides a summary of most recent advances and trends in automotive safety, especially related to Automated Driving Systems (ADS). It covers both functional safety, safety of the intended functionality (SOTIF) and their relationships with other areas of dependability such as cybersecurity. It also covers the several standardization activities currently ongoing in safety and Artificial Intelligence. The paper mostly focuses on HW

but it also describes the major challenges related to HW-SW interface.

01:55 p.m.
7C.2 - Thermal-Neutron SER Mitigation by Cobalt-Contact in 7 nm Bulk-FinFET Technology, Taiki Uemnrct, Byiingjin Chung, Jegon Kim, Hvewon Shim, Shinyoung Chung, Brandon Lee; Samsung Foundry, Samsung Electronics, Jaehee Choi; Semiconductor Research and Development Center, Shota Ohnishi, Ken Machida; Samsung Research and Development Institute Japan

This paper presents thermal-neutron soft error rates (tnSER) in 7 nm bulk-FinFET technology with applied Cobalt (Co) contact. A thermal-neutron irradiation test at MURR shows tnSER reduction in the 7 nm: the tnSER in the 7 nm (Co-contact) is 0.0012X of the tnSER in 14 nm (Tungsten (W)-contact). Simulation analysis shows that tnSER changed by 0.21X due to the advancement of transistor technology (from 14nm to 7nm) and 0.0057X due to the change in contact-material (from W to Co).

02:20 p.m.
7C.3 - Soft Error Characterization of D-FFs at the 5-nm Bulk FinFET Technology for the Terrestrial Environment, Y. Xiong, A. Feeley, N.J. Pieper, D.R. Ball, B.L. Bhuva; Vanderbilt University, B. Narasimham; Broadcom Inc, J. Brockman, University of Missouri Research Reactor, N.A. Dodds, Sandia National Laboratories, S.A. Wender, Los Alamos National Laboratory, S.-J. Wen, R. Fung; Cisco Systems Inc.

Soft error rates (SER) are characterized for the 5-nm bulk FinFET D flip-flops for alpha particles, thermal neutrons, and high-energy neutrons as a function of supply voltage. At nominal operating voltage, the 5-nm node has higher SER than the 7-nm node for all three particle types, with increases of 148%, 168%, and 26%, respectively. The overall SER for the 5-nm node was ~2X greater than that of the 7-nm node, because the reduction in critical charge was higher than that in collected charge. For alpha particle exposures, temperature effects on SER were more prominent for the 5-nm node than both the 7-nm and 16-nm node. Relative contribution of alpha particle SER increases with scaling, and it accounts for 13% of the overall SER at the 5-nm node.

7C - Authors' Corner
Wednesday, March 30, 02:45 p.m. – 03:05 p.m. CDT

8A – Intro
Wednesday, March 30, 03:05 p.m. – 03:10 p.m. CDT

8A - PR (Product Reliability)
Wednesday, March 30, 03:10 p.m. – 05:15 p.m. CDT
Venue: International I & II

03:10 p.m.
8A.1 (Invited) - Reliability Qualification Challenges of SOCs in Advanced CMOS Process Nodes, Shou-En Liu, Jian Li, Deepak Nayak, Amit Marathe; Silicon Reliability, Product Integrity Engineering, Kaushik Balamukundhan, Vishal Gosavi, Ajaykumar Prajapati, Baha Kilic, Mengzhi Pang, Arpit Mittal; Silicon Design, Consumer Hardware, Google Inc.

We discuss the reliability methodology and risk mitigation for qualification and reliability of SOCs in advanced Finfet technology nodes. Determining SOC mission profile through field data collection is demonstrated from a practical case as a first step towards developing an efficient qualification methodology. The challenges of HTOL testing in advanced process nodes are discussed and the mitigation methodology is presented. It is shown that an accurate mission profile is of paramount importance to achieve target lifetime and FIT from the HTOL testing. Finally, the influence of new package technology on the reliability qualification SOCs is analyzed via FEA simulation and board-level reliability experimental data.

03:35 p.m.
8A.2 - Runtime Test Solution for Adaptive Aging Compensation and Fail Operational Safety mode, Vincent Huard, Souhir Mhira, Lionel Jure, Olivier Montfort; Dolphin Design, Paolo Bernardi; Politecnico di Torino

This paper is demonstrating for the first time a full, industrial-grade, DFT-based approach in 22FDX node combining PVT and Aging compensation, with runtime test solution for hard events detection (TDDB, EMG,..) and Fail Operational mode for compliance with 2018 version of ISO26262 norm.

04:00 p.m.
8A.3 - New RC-Imbalance Failure Mechanism of Well Charging Damage and The Implemented Rule, Yu-Lin Chu, Hsi-Yu Kuo; Quality & Reliability, Hung-Da Dai, Kuan-Hung Chen, Pei-Jung Lin, Chun-Ting Liao, Ta-Chun Lin, Swercy Chiu, Victor Liang; Product Engineering, Ming Feng; DRC

In this paper, a new failure model that explains the plasma-induced damage (PID) involving two wells is described. Contrary to common explanation that the larger wells discharge and damage devices in smaller wells, we propose that the damage is caused by an imbalance of the "RC" associated with each "well system". The victim gate can reside in either the large or small well. This RC imbalance model is supported by the results of various test patterns designed in a 0.13um BCD (Bipolar-CMOS-DMOS) process using NBL (N-type Buried Layer). New design rules have been developed based on the test pattern results.

04:25 p.m.
8A.4 - A Method of Developing Qualification Plans for Board Products, Jeffrey Zhang, Antai Xu, Daniel Gitlin; Xilinx Inc., 2100 Logic Drive

The semiconductor industry has well-established standards to qualify integrated circuits (IC), but the situation is quite different with qualifying board products. IPC-9701 is often referred to when evaluating board level reliability (BLR), but IPC-9701 doesn't have clearly defined pass/fail criteria, and it is mostly intended for evaluating BLR performance of a single IC, not for complex functional board products such as expensive PCIe accelerator cards. This study presents a method of developing cost-effective qualification plans for board products by analyzing ~45 board temperature cycle (TC) runs.

04:50 p.m.
8A.5 - Reduced Relative Humidity (RH) Enhances the Corrosion-Limited Lifetime of Self-Heated IC: Peck's Equation Generalized, M. Asaduz Zaman Mamun, Muhammad A. Alam; Department of ECE, Purdue University

Since the early 1980s, highly accelerated stress tests (HAST) have been used as an industry-standard method to qualify the correlated moisture-enhanced, and temperature-accelerated electrochemical bond wire failures of non-hermetically packaged Integrated Circuits (IC). In this regard, empirical Peck's equation has traditionally been used to translate the HAST failure rates to the corresponding failure rates under application-specific use conditions. Unfortunately, this use-condition lifetime projection is challenging because self-heated ICs correlate relative humidity *(RH)* and temperature *(T)* in a way that is not explicitly accounted for by Peck's equation. Here, we develop a predictive and self- consistent reliability modeling tool that: (i) explicitly accounts for the intermittent IC self-heating data collected from laptop/device/cellphone users', moisture ingress in the filler tunable epoxy molding compounds (EMCs), and Cu-Al bond wire corrosion in an integrated way; (ii) demonstrates how the asymmetry between on and off-state heating leads to dramatic suppression of the effective *RH* experienced by an integrated circuit; and most importantly, (iii) identifies that the corrosion of Cu-Al bond wire occurs in spikes during the on-off transition when both *RH* and *T* are high. Our integrated, self-consistent predictive Multiphysics model provides deep insights into the Cu-Al bond wire failure and suggests a pathway to application-aware Generalized Peck's equation relevant for self-heated ICs under arbitrary operating conditions.

8A - Authors' Corner

Wednesday, March 30, 05:15 p.m. – 05:35 p.m. CDT

8B – Intro
Wednesday, March 30, 03:05 p.m. – 03:10 p.m. CDT

8B - WB (Wide-Bandgap Semiconductors (SiC)
Wednesday, March 30, 03:10 p.m. – 05:15 p.m. CDT
Venue: International III & IV

03:10 p.m.
8B.1 - Negative Gate Bias TDDB evaluation of n-Channel SiC Vertical Power MOSFETs, Satyaki Ganguly, Daniel J. Lichtenwalner, Caleb Isaacson, Donald A. Gajewski, Philipp Steinmann, Ryan Foarde, Brett Hull, Sei-Hyung Ryu, Scott Allen, John W. Palmour; Wolfspeed, Inc.

With the steep expansion of the n-type 4H-SiC power metal-oxide-semiconductor field-effect transistor (MOSFET) market space, gate oxide reliability is gaining more and more attention. Although there exist several reports dealing with the bias temperature instability (BTI) under both positive and negative gate biases, gate oxide lifetime evaluations predominantly focus on positive gate bias time-dependent dielectric breakdown (TDDB) stresses for n-channel SiC MOSFETs. In this work we address that gap. From the negative gate bias TDDB data measured at 175 °C and at a gate oxide electric field of about 4 MV/cm, an intrinsic lifetime of 1E8 hours has been predicted, which closely matches with the results obtained from similar devices under positive gate stress. Also, in this work the correlation between failure location in a MOSFET unit cell and the failure signatures during TDDB stress have been established, and an explanation from a device physics standpoint has been provided. The identification of the failure location in the unit cell from in-situ gate leakage data without the need of physical failure analysis can turn out to be key during the early phase of a new process development activity.

03:35 p.m.
8B.2 - Accurate screening of defective oxide on SiC using consecutive multiple threshold-voltage measurements, H. Miki, M. Sagawa, Y. Mori; Center for Technology Innovation - Electrification Hitachi, T. Murata, K. Kinoshita, K. Asaka, T. Oda, Hitachi Power Semiconductor Device

A high rate of early failures in gate oxide is one of the most serious concerns regarding the reliability of silicon carbide metal-oxide-semiconductor field-effect transistors. An intensive screening test using high-voltage gate stress is key to reducing this rate. However, a threshold-voltage (V_{TH}) shift is a frequent side effect, and the degraded chips need to be eliminated.
We propose a screening procedure to detect adverse degradation with improved accuracy. We first analyzed the V_{TH} hysteresis, which deteriorates the measurement accuracy of V_{TH} shifts and found that its wide variation is due to several causes. We thus investigated multiple consecutive V_{TH} measurements to isolate the hysteretic component from data and confirmed that our procedure is highly useful in detecting the adverse VT_H shift. In particular, it can identify a negative VT_H shift hidden by the hysteresis. This procedure is advantageous for negative-voltage screening in which small gate leakage can alter its V_{TH}.

04:00 p.m.
8B.3 - Investigation of Terrestrial Neutron Induced Failure Rates in Silicon Carbide JFET Based Cascode FETs, L. Fursin, P. Losee; Qorvo, 650 College Road East, A. Akturk; CoolCAD Electronics, LLC, 5000 College Avenue, Suite 2105

The terrestrial Neutron failure rate of SiC JFETs and JFET based Cascode FETs are investigated for the first time. The contributions of the co-packaged low voltage Si MOSFETs within the Cascode FETs were found to be insignificant in the overall FIT of the high-voltage switches. Meanwhile, the SiC JFET and resulting Cascode FETs were found to be comparable with the previously reported "Universal" behavior of SiC unipolar devices when analyzed as FIT/cm^2 versus applied voltage when normalized to device breakdown voltage. These results suggest that, due to their superior specific on-resistance ($R_{DS,ON}$ x Active Area), SiC JFETs and Cascode FETs will

offer lower terrestrial FIT for a given on-resistance.

04:25 p.m.
8B.4 (IIRW BSP) - Understanding the Reliability of Ferroelectric Tunnel Junction Operations using an Advanced Small-Signal Model, Lorenzo Benatti; Unimore

Ferroelectric technology is becoming ever more appealing for a variety of applications, especially analog neuromorphic computing. In this respect, elucidating the physical mechanisms occurring during device operation is of key importance to improve the reliability of ferroelectric devices. In this work, we investigate ferroelectric tunnel junctions (FTJs) consisting of a ferroelectric hafnium zirconium oxide (HZO) layer and an alumina (Al2O3) layer by means of C-f and G-f measurements performed at multiple voltages and temperatures. For a dependable interpretation of the results, a new small signal model is introduced that goes beyond the state of the art by i) separating the role of the leakage in the two layers; ii) including the significant impact of the series impedance (that depends on the samples layout); iii) including the frequency dependence of the dielectric permittivity; iv) accounting for the fact that likely not the whole HZO volume crystallizes in the orthorhombic ferroelectric phase. The model correctly reproduces measurements taken on different devices in different conditions. Results highlight that the typical estimation method for interface trap density may be misleading.

04:50 p.m.
8B.5 (ESREF BP) - Evaluation of Thermomechanical Fatigue Lifetime of BGA Lead-Free Solder Joints and Impact of Isothermal Aging, Pierre Roumanille, Emna Ben Romdhane, Samuel Pin; IRT Saint Exupéry, Patrick Nguyen; Elemca, Jean-Yves Delétage, Alexandrine Guédon-Gracia, Hélène Frémont; IMS Laboratory

The present work aims at investigating how the BGA solder fatigue life in thermal cycling is affected by prior isothermal aging. The Weibull distributions of SAC305 assemblies are considered through failure analysis and microstructural investigations. The main metallurgical effect of isothermal aging observed on solder joints is a strong coalescence of precipitates. The fatigue life was slightly lowered by an extended aging at 100°C while exposure at 150°C proved to increase it. Tin recrystallization and strain-enhanced precipitate coarsening led to intergranular cracking in the solder joints, which was the main failure mode. However, cracking in the PCB laminate was also noticed and mainly present in failed specimens that were previously aged at 150°C. The prior degradation of the board material near its glass transition temperature and the lower stress in the solder joints due to laminate cracking were proposed to explain the unexpected lifetime extension.

8B - Authors' Corner
Wednesday, March 30, 05:15 p.m. – 05:35 p.m. CDT

8C – Intro
Wednesday, March 30, 03:05 p.m. – 03:10 p.m. CDT

8C - MB (Metallization/BEOL Reliability)
Wednesday, March 30, 03:10 p.m. – 05:15 p.m. CDT
Venue: Cap Rock I, II & III

03:10 p.m.
8C.1 (Invited) - Novel Methodology for Temperature-Aware Electromigration Assessment in On-Chip Power Grid: Simulations and Experimental Validation, A. Kteyan; Siemens EDA, Yerevan, V. Sukharev; Siemens EDA, Fremont, Y. Yi, C. Kim; Dept. of ECE, University of Minnesota

A novel methodology for electromigration (EM) failure assessment in power/ground nets of integrated circuits, which is based on analysis of IR drop degradation, has been enhanced by considering non-uniform temperature distribution in interconnects. Temperature gradient along an interconnect tree can affect void nucleation due to the divergency of atomic flux, as well as due to development of thermal stress. Compact models for resistance

increase of voided metal have been developed, using results of FEM simulations of voiding kinetics in via-metal structures. The simulation approach has been validated using measurements of node voltages in a specially designed test power grid. Increase of anode-cathode voltage drop above a threshold value was adopted as a failure criterion determining time-to-failure (TTF) of the grid and mean-time-to- failure (MTTF) was obtained, assuming random distributions of the critical stress and atomic diffusivity. In the studied cases of temperature distributions, a good agreement of simulated and measured TTF distributions has been obtained.

03:35 p.m.
8C.2 - Assessment of Critical Co Electromigration Parameters, O. Varela Pedreira, M. Lofrano, H. Zahedmanesh, Ph. J. Roussel, V. Simons, E. Chery, I. Ciofi, K. Croes; Advanced Reliability Robustness and Test, M. van der Veen; imec

We perform a detailed assessment of the electromigration performance of Co interconnects. Package level EM measurements were performed during >11 months. Our estimate of the EM activation energy is ~1.4 eV which is, within error bar, consistent with earlier reported numbers. Our current exponent estimate suggests that void growth is the dominant contributor to Co EM. Through failure analysis, we associate void growth occurring through grain boundaries and at the barrier/metal interfaces. An activation energy assessment using low frequency noise measurements suggest a stronger contribution from this latter interface. Finally, we make a first estimation of an effective DoZ* for Co of ~1.72×10-10 which is two orders of magnitude lower than for Cu.

04:00 p.m.
8C.3 - Redundancy Effect on Electromigration Failure Time in Power Grid Networks, M. H. Lin, C. I. Lin, Y. C. Wang, Aaron Wang; Taiwan Semiconductor Manufacturing Company. Ltd.

We characterize the redundancy effect on EM failure time in power grid networks and propose a flow to leverage the benefit of the redundancy effect on EDA tools. Experimental results fit Monte-Carlo simulation based on a parallel model incorporating time-dependent stress loading. Ring oscillator frequency degradation and clock tree time delay are also evaluated on simplified power mesh networks as EM voids occur. A simple and practical EM check algorithm for EDA tools that takes the benefit of the redundancy effect on power grid networks into account is proposed.

04:25 p.m.
8C.4 - Polarity Dependence and Metal Density Impact on Multi-Layer Inter-Level TDDB for High Voltage Application, Yinghong Zhao, Ki-Don Lee, Manisha Sharma, Joonah Yoon, Rakesh Ranjan, Iqbal Mahmud, Caleb Dongkyan Kwon; Samsung Austin Semiconductor, Myung Soo Yeo; Samsung Foundry Business

For high voltage application at a fixed inter-metal distance, dielectric reliability has been investigated on multi-layer inter-level interconnects, focusing on conduction mechanism and geometry effect. From Vramp (voltage-ramp-to-breakdown) tests, Vbd is found to be 4-5% lower with positive bias applied to the bottom metal, which is believed to be due to the polarity- dependent conduction mechanism. IV characteristics of two different bias configurations at various temperatures suggest that Poole-Frenkel and Fowler-Nordheim, respectively, dominates for a high bias to the bottom and top electrodes. In addition, metal density affects the lifetime of inter-level TDDB (time dependent dielectric breakdown) with Poisson area scaling. Based on our studies, a guideline for additional reliability margin can be proposed by bias polarity restriction and layout design optimization.

8C - Authors' Corner
Wednesday, March 30, 05:15 p.m. – 05:35 p.m. CDT

Taste of Texas Poster Dinner
Wednesday, March 30, 06:00 p.m. – 09:00 p.m. CDT
Venue: Austin Ranch

P1 - Reliability Analysis of Physically Unclonable Function by using Aging Variability Simulation, Jae-Gyung Ahn, Jim Wesselkamper, Ryan SW Baek, Ping-Chin Yeh, Jonathan Chang, Jennifer Wong, Xin Wu; Xilinx Inc

We applied Monte Carlo (MC) aging simulation flow to explain measured aging effects of PUF (Physically Unclonable Function) circuit. Simulation data provides a good understanding of how PUF circuit stability is degraded with the NBTI effect. Procedure of using MC aging simulation flow to predict PUF stability is explained in detail. Result from simulation is well matching with the measured data when the variability model is correctly extracted considering MOSFET device size. This flow was used to predict the stability of different types of PUF designs.

P2 - A Calibration - Free Synthesizable Odometer Featuring Automatic Frequency Dead Zone Escape and Start - up Glitch Removal, Tahmida Islam, Junkyu Kim, Chris H. Kim; Department of Electrical and Computer Engineering, University of Minnesota, David Tipple, Michael Nelson, Robert Jin, Anis Jarrar; NXP Semiconductors

This paper presents a synthesized version of the silicon odometer aging sensor for measuring the frequency degradation caused by device degradation mechanisms in high volume semiconductor products. In the design, three ring oscillators (ROSCs) composed of inverter, NAND, and NOR gates are implemented in register-transfer-level (RTL), with the ability to be stressed in an AC or DC stress condition. The new odometer has product level features such as calibration-free operation, automatic frequency dead zone escape, and start-up glitch removal. The odometer verilog code was synthesized and automatically placed-and-routed in three different technologies using standard ASIC design tools. As a proof of concept, we show aging data collected from a 65nm test chip with 12 synthesized odometer instances. The open-source RTL files and testbench of the synthesizable odometer can be downloaded from https://github.com/reliability-research/odometer.

P3 - A Smart SRAM-Cell Array for the Experimental Study of Variability Phenomena in CMOS Technologies, P. Saraza-Canflanca, H. Carrasco-Lopez, A. Santana-Andreo, R. Castro-Lopez, E. Roca, F. V. Fernandez; Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC/Universidad de Sevilla), J. Diaz-Fortuny; imec

Time-Dependent Variability phenomena can have a considerable impact on circuit performance, especially for deeply-scaled technologies. To account for this, these phenomena need to be characterized and modelled. Such characterization is often performed at the device level first. Then, the model extracted from such characterization should be validated at the circuit level. To this end, this paper presents a novel chip fabricated in a 65-nm technology that contains an array of 6T SRAM cells. This chip includes some features that make it especially adequate for the characterization of the impact of Time-Dependent Variability phenomena. To demonstrate this adequacy, different tests have been performed to evaluate how Time-Dependent Variability phenomena impact several relevant performance metrics of SRAM cells.

P4 - An Aging Degradation Suppression Scheme at Constant Performance by Controlling Supply Voltage and Body Bias in a 65 nm Fully-Depleted Silicon-On-Insulator Process, Kazutoshi Kobayashi, Ikuo Suda; Department of Electronics, Graduate School of Science and Technology, Kyoto Institute of Technology, Ryo Kishida; Department of Electrical Engineering, Faculty of Science and Technology, Tokyo University of Science

We propose an aging degradation suppression scheme at constant performance by controlling supply voltage and body bias for an FDSOI device. Reducing supply voltage while increasing body bias can maintain performance and suppress dynamic power and aging degradation caused by BTI. From measurement results of ring oscillators in a 65 nm FDSOI, PBTI- and NBTI-induced degradations can be reduced by 71% and 66% at 1.5 V supply voltage and 0.20 V forward body bias paying the penalty of 3.03x static power increase. From simulation results by a 16-bit ALU, the figure of merit defined by the product of the time exponent **n** from NBTI, static and dynamic power consumption becomes almost constant at any body bias.

P5 - Cleaved-Gate Ferroelectric FET for Reliable Multi-Level Cell Storage, Navjeet Bagga; Department of Electronics and Communication Engineering, Kai Ni; Microsystems Engineering Rochester Institute of Technology, Nitanshu Chauhan; Department of Electronics Engineering, Om Prakash; Karlsruhe Institute of Technology, X. Sharon Hu; University of Notre Dame, Hussam Amrouch; Chair of Semiconductor Test and Reliability (STAR)

A novel Ferroelectric FET (FeFET) structure to enable reliable multi-level cell (MLC) storage using a cleaved gate (CG) is proposed for the first time. The CG-FeFET features a gate that is cleaved into two regions separated by an insulator. Cleaving off the gate modulates the channel conductance, and in turn, memory window (MW) and sense margin, i.e., the ratio of I_D measured for LOW-V_T and high-V_T states [$(I_D)_{LVT}/(I_D)_{HVT}$]. The proposed CG-FeFET is investigated and optimized based on well- calibrated TCAD models. We perform an extensive design space exploration in order to evaluate: 1) the impact of the length of separation oxide (L_{OX}) inserted between the source side gate (G_S) and the drain side gate (G_D); 2) whether reading from G_S or G_D is better, and 3) the best placement of the insulator between the two gates comparing *symmetric* ($L_{G\_S}=L_{G\_D}$) vs. *asymmetric* ($L_{G\_S}\neq L_{G\_D}$) structures. Our investigations provide detailed guidelines for designing a CG-FeFET that exhibits 3x larger MW and 6.6x higher $(I_D)_{LVT}/(I_D)_{HVT}$ compared to the baseline FeFET. Such significant improvements offered by CG-FeFET greatly increase the noise margin of the FeFET device; thus, storing four different states with an order of magnitude distinguishable sensing current. Hence, *two bits can be reliably stored* in CG-FeFET, opening the door for reliable MLC-FeFETs.

P6 - Combining Experiments and a Novel Small Signal Model to Investigate the Degradation Mechanisms in Ferroelectric Tunnel Junctions, Lorenzo Benatti, Paolo Pavan, Francesco Maria Puglisi; Dipartimento di Ingegneria "Enzo Ferrari", Via P. Vivarelli 10/1, 41125 - Modena (MO)

Ferroelectric emerging memories have been found to perfectly act as ultra-low power synaptic weights but require a deeper investigation before their actual introduction in brain inspired computing platforms. In particular, the understanding of the physical mechanisms occurring during the lifetime of the ferroelectric tunnel junction memories is fundamental for the development of reliable neuromorphic circuits. In this respect, in this work we combined an extended stress/measure sequence and a newly proposed and validated small signal model to provide insights on the degradation mechanisms occurring in these devices. The model considers the known voltage and frequency dependence of the material properties, the impact of the interface and bulk traps, and separates the leakage contributions of the layers. Results reveal that reliability is ultimately limited by the *defect generation in the ferroelectric* with stress. Asymmetry in the polarization-dependent leakage increase (due to defect generation) is found, that is associated with the different stages (wake-up, fatigue, aging) of the device lifetime. Suggestions on the possible optimization of the pulse design for improving the useful lifetime of the device are also reported.

P7 - Endurance Evaluation on OTS-PCM Device using Constant Current Stress Scheme, W.C. Chien, C.H. Yang, C.W. Yeh, H.Y. Cheng, I T. Kuo, E.K. Lai, C.S. Hsu, H.L. Lung; IBM/Macronix Phase Change Memory Joint Project, Y.C. Chou, H.Y. Ho; Product Design and Engineering Center, L.M. Gignac, N. Gong, W. Kim, C.W. Cheng, L. Buzi, A. Ray, R.L. Bruce, M. BrightSky; IBM T.J. Watson Research Center

A constant current stress scheme is implemented for endurance study on OTS-PCM devices for the first time. It provides a feasible method to estimate the read/write endurance for cross-point PCM products, which can save testing time for chips qualification. A 256kb chip with 1E7 cycles is demonstrated that corresponds with the endurance evaluation on the doped AsGeSe OTS with doped $Ge_2Sb_2Te_5$ system.

P8 - Experimental Demonstration of Single-Level and Multi-Level-Cell RRAM-Based In-Memory-Computing with up to 16 Parallel Operations, E. Esmanhotto, T. Hirtzlin, N. Castellani, S. Martin, F. Andrieu, J.F. Nodin, E. Vianello; CEA-Leti, Université Grenoble Alpes, B. Giraud; CEA-List, Université Grenoble Alpes, D. Querlioz; Université Paris-Saclay, CNRS, C2N, Palaiseau, J-M. Portal; Aix-Marseille Université, IM2NP, Marseille

Crossbar arrays of resistive memories (RRAM) hold the promise of enabling In-Memory Computing (IMC), but essential challenges due to the impact of device imperfection and device endurance have yet to be overcome. In this work, we demonstrate experimentally an RRAM-based IMC logic concept with strong resilience to RRAM variability, even after one million endurance cycles. Our work relies on a generalization of the concept of in-memory Scouting Logic, and we demonstrate it experimentally with up to 16 parallel devices (operands), a new milestone for RRAM in-memory logic. Moreover, we combine IMC with Multi-Level-Cell programming and demonstrate experimentally, for the first time, an IMC RRAM-based MLC 2-bit adder.

P9 - Correlation between Access Polarization and High Endurance (~ 1012 cycling) of Ferroelectric and Anti-Ferroelectric HfZrO2, K.-Y. Hsiang; Institute and Undergraduate Program of Electro-Optical Engineering & Department of Electronics Engineering and Institute of Electronics, C.-Y. Liao, Y.-Y. Lin, Z.-F. Lou, C.-Y. Lin, J.-Y. Lee, F.-S. Chang, Z.-X. Li, H.-C. Tseng, C.-C. Wang, W.-C. Ray, M. H. Lee; Institute and Undergraduate Program of Electro-Optical Engineering, T.-H. Hou ; Department of Electronics Engineering and Institute of Electronics, T.-C. Chen, C.-S. Chang; Corporate Research, Taiwan Semiconductor Manufacturing Company

Endurance ~10^{12} cycling of ferroelectric (FE) and antiferroelectric (AFE) $HfZrO_2$ (HZO) capacitors are achieved experimentally by adjusting the programming pulse width (t_p). The correlation between switching polarization (ΔP) and fatigue behavior of high endurance is discussed. For long t_p (= 1 μs), AFE exhibits excellent endurance with > 10^{10} cycles as compared with FE ~ 10^9 cycles. With shortening t_p, the endurances of FE and AFE are significantly improved. There is no significant degradation until > 10^{11} cycling is observed for FE with t_p=20ns.

P10 - Degradation Mechanism of Amorphous IGZO-Based Bipolar Metal-Semiconductor-Metal Selectors, Taras Ravsher, Jan Van Houdt; Department of Physics and Astronomy & imec, Andrea Fantini, Adrian Vaisman Chasin, Shamin Houshmand Sharifi, Hubert Hody, Harold Dekkers, Thomas Witters, Sebastien Couet, Gouri Sankar Kar; imec, Valeri Afanas'ev; Department of Physics and Astronomy

To enable high-density cross-point arrays of magnetic memory a suitable access device is necessary. A promising candidate for this role is a metal-semiconductor-metal (MSM) tunneling device. In this work, the operation of an ultrathin Pt\6nm a-IGZO\Pt stack as an MSM selector is discussed. The focus is given to understanding the breakdown mechanism at high current regime, which prevents it from reaching the target current density. The breakdown is preceded by a gradual degradation process, which is manifested as an increase in high- field current after prolonged stress. This effect is recoverable - current returns to original value after sufficient delay time. Based on these observations, we propose a mechanism, where increased high-field current can be explained as a decrease in Schottky barrier height arising from stress-induced increase in oxygen vacancies.

P11 - Impact of Temperature on Reliability of MFIS HZO-Based Ferroelectric Tunnel Junctions, Ayse Sünbül, Tarek Ali, Raik Hoffmann, Ricardo Revello, Yannick Raffel, David Lehninger, Kati Kühnel, Matthias Rudolph, Sebastian Oehler, Philipp Schramm, Malte Czernohorsky, Konrad Seidel, Thomas Kämpfe; Fraunhofer Institute for Photonic Microsystems IPMS, Center Nanoelectronic Technologies (CNT), Pardeep Duhan; Department of Electrical Engineering, Indian Institute of Technology (IIT) Ropar, Lukas M. Eng; Institut für Angewandte Physik, Technische Universität Dresden & Center of Excellence, Complexity and Topology in Quantum Matter ct.qmat: Dresden-Würzburg Cluster of Excellence-EXC 2147

Hafnium oxide-based ferroelectric tunnel junctions (FTJs) are novel nonvolatile memory devices with promising advantages such as non-destructive readout in comparison to conventional ferroelectric random access memories (FRAMs). Reliability aspects of FTJ devices need to be investigated, including their endurance, retention, ferroelectric switching, breakdown characteristics, and memory window (MW). These characteristics exhibit promising results at room temperature; however, further analysis is required for different operating temperatures. Therefore, in this work, we demonstrate the FTJ device characteristics at different temperatures varying from -40 °C to 60 °C. The results indicate that high temperatures cause higher MW of FTJs, whereas the FTJ lifetime increases at lower operating temperatures.

P12 - Trap-Polarization Interaction during Low-Field Trap Characterization on Hafnia-Based Ferroelectric Gatestacks, B. Truijen, B. O'Sullivan, P. Roussel, A. Chasin, G. Van den Bosch, B. Kaczer ; imec, Md Nur K. Alam, D. Claes; imec & KU Leuven, Department of Materials Engineering, M. Thesberg; Global TCAD Solutions GmbH, Vienna, Austria, formerly: Institute for Microelectronics, J. Van Houdt; imec & KU Leuven, Department of Physics and Astronomy

This paper investigates the characterization of charge trapping and its modelling on hafnia-based ferroelectric field effect transistors (FeFETs). Defect characterization on MOSFETs can be done by studying threshold voltage shifts (ΔVth) as a function of charging and relaxation times. At positive gate voltages one expects electron trapping in the gate oxide to result in a positive shift of the threshold voltage (Vth). However, on a FeFET those conditions will induce polarization changes in the gate oxide leading to a negative Vth-shift, complicating the characterization of defect levels. We aim to alleviate these difficulties by modelling the polarization and trapping in FeFETs over a wide range of timescales, suitable for defect characterization. We demonstrate quantitative agreement on long timescales with a static polarization model, while a time- dependent polarization model can be used for qualitative agreement over a wide range of times from 30 ms to 2 ks.

P13 - Characterization and Analysis of RF Switches in SOI Technology for ESD Protection, Jian Liu, Nathaniel Peachey; ESD Engineering, Qorvo Inc., Nathaniel Carels; Department of Electrical and Computer Engineering, North Carolina State University

The self-protection of SOI RF switches is presented in this paper. TLP ESD test results show that the ESD protection performance of SOI RF switches is impacted by various parameters, including switch array gate channel length, finger width, finger number, and RF switch stack number. The physics of the SOI RF switch ESD protection mechanism is also studied by comparing TLP ESD test results from SOI RF switch splits and other ESD protection structures. It is concluded that the SOI RF switch self-protection process during ESD transients contains two mechanisms: NMOS channel conduction triggered by gate coupling effect and parasitic bipolar turning on.

P14 - Voltage Surges by Backside ESD Impacts on IC Chip in Flip Chip Packaging, Takuya Wadatsumi, Kohei Kawai, Rikuu Hasegawa, Takuji Miki, Makoto Nagata; Graduate School of Science, Technology, and Innovation, Kobe University, Kikuo Muramatsu; e-SYNC Co., Ltd., Kyoto, Hiromu Hasegawa, Takuya Sawada, Takahito Fukushima, Hisashi Kondo, MegaChips Corp., Osaka

Voltage surges induced by electrostatic discharge (ESD) impacts on the backside of an integrated circuit (IC) chip in flip-chip packaging potentially causes reliability problems and even leads to malfunctioning. On-chip voltage waveform monitor circuits on its frontside evaluate the surge as high as 200 mV when ESD gun at 200 V is discharged to the Si substrate backside through the contact resistance of 5 kΩ to the backside of a 350 μm thick Si substrate. The distribution of voltages over the frontside area of an IC chip is measured and explained with full-system level backside ESD simulation.

P15 - A Novel Latch-Up-Immune DDSCR Used for 12 V Applications, Zhihua Zhu, Songyan Wang, Xiaomei Fan; School of Information Engineering, Zhengzhou University, Zhengzhou

In this paper, a high holding voltage dual-directional silicon-controlled rectifier (SCR) with an embedded shunt path (HVDDSCR-ESP) for high-voltage I/O electrostatic discharge (ESD) protection is proposed. Based on the 0.13-μm BCD process, multi-current pulses that mimic the transmission line pulse (TLP) are applied to devices by using Sentaurus-TCAD. The results reveal that the proposed structure, compared with the conventional low-trigger dual directional SCR (LTDDSCR), has adjustable high holding voltage and good ESD robustness. In addition, the working mechanisms are also investigated, and the proposed device as the ESD cell is beneficial for the 12V applications and has no risk of latch-up.

P16 - Numerical Simulation and Characterization of PCB Warpage, M. Hamid, K. O'Connell, J. Bielick, J.

Bennett, E. Campbell, A. Alfoqaha; IBM

In this work an implicit finite element model of a Printed Circuit Board (PCB), connectors, and stiffener is developed. The effect of several parameters on the strain distribution on the board was analyzed. The PCB was bolted to an aluminum stiffener. The simulation went through several steps to consider the effect of the solder reflow process as well as bolt pretention forces and plug-in forces of the connectors. Based on the simulation, board warpage and bolt pretention forces had significant effect on board strain.

P17 - Adhesion-Limit in Refractory Transition Metal (Mo) Contact Relay Operation at 300 °C— Avoiding Implicated Overestimation for Modern ICs, Sushil Kumar, Dhairya Singh Arya, Manu Garg, Pushpapraj Singh; Centre for Applied Research in Electronics, Indian Institute of Technology Delhi

Micro-electromechanical relays with lower switching voltage are always a promise. In such relay, switching operation requires not only stable contact but also a reliable opening of the closed contacts. Therefore, stability against operational collapsing is another important reliability issue. Thus, a collapsing-free relay is always a challenging requirement. In this article, our core idea is to overcome this challenge. Herein, a systematic experimental and theoretical evaluation of limiting adhesion between refractory metal (Mo) is presented for a range of temperatures. The established framework allows direct and error-free extraction of F_{vdw} from measured data. This work has the potential to be used both as an in-line wafer-level testing (WLT) in foundries and for monitoring the device functionality after packaging when it comes to adhesion characterization.

P18 - Single Event Induced Crosstalk of Monolithic 3D Circuits Based on a 22 nm FD-SOI Technology, Junjun Zhang, Fanyu Liu, Bo Li, Yang Huang, Siyuan Chen, Yuchong Wang, Jiajun Luo, Key Laboratory of Science and Technology on Silicon Devices, Institute of Microelectronics, Jing Wan; State key lab of ASIC and System, School of Information Science and Technology, Fudan University

The single event induced crosstalk of monolithic 3D (M3D) integrated inverter chain is investigated using GEANT4 and TCAD simulations from layout, spacing, length, supply voltage and transistor size. The accurate ionization profiles are initially obtained and modelled in TCAD. Meanwhile, the crosstalk capacitances between interconnect lines or transistors are acquired through 3D simulation. Results show that the crosstalk pulse is closely related to interconnect length and peaks at 50 μm for transistor-level M3D. Vertical alignment of PMOS and NMOS in two inverter chains (gate level) respectively on different tier is the optimal layout to mitigate the single event induced crosstalk pulse (5.9 ps and 130 mV). In addition, increasing thickness of inter-layer dielectric is the best way to eliminate the crosstalk effect nearly without area penalty, which is the intrinsic advantage compared to planar circuits.

P19 - Failure Analysis of AlGaN/GaN Power HEMTs through an Innovative Sample Preparation Approach, R. L. Torrisi, S. Adamo, S. Alessandrino, C. Bottari, B. Carbone, M. Palmisciano, E. Vitanza; STMicroelectronics

This work shows an approach to carry out the de- layering, through a series of smart solutions, of the die surface of AlGaN/GaN HEMT with 3 metal levels plus Cu-RDL, after to have performed Fault Localization in the best way - from resolution and wavelengths detection point of view - from the backside of the device without Silicon substrate, that means the final die thickness is ~ 7μm. This approach allows advanced physical analysis on AlGaN surface, observing at high resolution and magnification defective points and comparing them with other close areas, improving consistently the global information about the die surface.

P20 - Influence of Drain and Gate Potential on Gate Failure in Semi-Vertical GaN-on-Si Trench MOSFET, D. Favero, C. De Santi, K. Mukherjee, G. Meneghesso, E. Zanoni, M. Meneghini; Department of Information Engineering, University of Padova, K. Geens, M. Borga, B. Bakeroot, S. You, S. Decoutere; imec

In this work, a detailed analysis of degradation and failure of semi-vertical GaN-on-Si trench MOSFETs is

reported. OFF-state, semi-ON state and ON-state conditions were analyzed, to evaluate how the gate and drain bias can impact on the failure voltage. We demonstrate that: a) devices with a bilayer gate insulator (2.5 nm AhO3 interface dielectric to GaN, + 35 nm SiO2 main dielectric) have a superior performance, compared to single-insulator (35 nm AhO3) samples; b) in a drain step-stress, the gate voltage (resulting in different operating regimes, OFF, semi-ON or ON-state) can significantly impact on the failure voltage of the devices; c) stress at high V_{GS} and/or V_{DS} may induce a significant shift in threshold voltage, which is stronger when the devices are stressed in the ON-state. The results - complemented by 2D simulations - provide a description of the factors limiting the breakdown robustness of GaN vertical transistors.

P21 - Impact of Gate Offset on PBTI of p-GaN Gate HEMTs, Ethan S. Lee, Jesús A. del Alamo; Microsystems Technology Laboratories, Massachusetts Institute of Technology, Jungwoo Joh, Dong Seup Lee, Analog Technology Development, Texas Instruments

We study Positive-Bias Temperature Instability (PBTI) of enhancement-mode Schottky Type p-GaN gate HEMTs with different gate stack geometry. In particular, we experimentally investigate the impact of the gate offset, the portion of the p-GaN layer in the gate stack that is not contacted by the gate metal. Our study reveals trapping-induced negative threshold voltage shifts after benign gate stress that are recoverable, consistent with the literature. At very high gate stress voltages, there is a permanent negative threshold shift consistent with a leakier gate-metal/p-GaN junction. However, for long gate offset length devices, a new PBTI mechanism with a permanent positive threshold shift arises at high gate stress voltages that is uniquely associated with the uncontacted offset region of the p-GaN layer. This implies that there is a trade-off between increasing the gate offset length to limit sidewall leakage and ensuring stable device performance. Our study further reveals the role that gate current continuity across both barriers in the gate stack of a p-GaN HEMT plays in setting up the gate electrostatics.

P22 - Accelerating the Recovery of p-Gate GaN HEMTs after Overvoltage Stresses, Joseph P. Kozak; Center for Power Electronics Systems, Virginia Polytechnic Institute and State University & Johns Hopkins University Applied Physics Laboratory, Qihao Song, Jingcun Liu, Yuhao Zhang, Ruizhe Zhang, Qiang Li; Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Wataru Saito; Research Institute for Applied Mechanics, Kyushu University

GaN high electron mobility transistors (HEMTs) have limited avalanche capability and withstand the surge energy through capacitive charging, which often causes significant voltage overshoot up to their catastrophic limit. This work explores the parametric shift and recovery of a commercial Schottky-type, p-gate GaN HEMT under repetitive, overvoltage switching stresses near its dynamic breakdown voltage. In particular, the device recovery under various temperatures is comprehensively studied, which allows the identification of the de-trapping dynamics and dominant trap energy levels for the first time. Devices were stressed in a clamped inductive switching circuit with 1-million surge energy cycles with a voltage overshoot reaching 1300 V. The parametric shifts showed a saturation and were found to be caused by holes generated in impact ionization. The device recovery was found to be accelerated by elevated ambient temperatures, and a hole-trap energy level of 0.52 eV was identified to dominate the parametric shift and recovery. These results suggest the significance of hole dynamics on the overvoltage robustness of p-gate GaN HEMTs near their dynamic breakdown voltage.

P23 - Impact of Random Spatial Fluctuation in Non-Uniform Crystalline Phases on Multidomain MFIM Capacitor and Negative Capacitance FDSOI, Nitanshu Chauhan, Sarita Yadav; National Institute of Technology Uttarakhand & IIT Roorkee, Chirag Garg, Amit Kumar Behera, Shashank Banchhor, Avirup Dasgupta, Arnab Datta, Sudeb Dasgupta, Anand Bulusu; IIT Roorkee, Kai Ni; Rochester Institute of Technology, Navjeet Bagga; PDPM IIIT Jabalpur

In this work, we explain the phenomena of ferroelectricity modulation in the ferroelectric (FE) layer due to the residing dielectric (DE) phase. This work also demonstrates the impact of random spatial fluctuation of DE phase for multidomain Metal-Ferro-Insulator-Metal (MFIM) capacitor and Negative Capacitance (NC) FDSOI FET. Using well-calibrated TCAD models, we found: 1) the presence of DE phase causes non- uniformity in the

polarization (P_{FE}) and potential (V_{FE}) inside the FE-layer; 2) non-uniformity in the P_{FE} modulates the average FE capacitance (C_{FE}) due to an increased FE domain interaction; 3) the increase in DE phases decreases the C_{FE}; 4) higher FE thickness (T_{FE}) with higher DE phase exacerbates the C_{FE} variation, thus, in NC region the PFE becomes direction-dependent; 5) larger DE grain sizes show higher bias directional dependency in the NC region; 6) variation of the coercive field (E_C) within the FE layer with DE phase, predominantly increases the bias directional dependency in the NC region and thereby introduces the higher reliability concerns for NC-FETs.

P24 - Effect of Non-Identical Annealing on the Breakdown Characteristics of Sputtered IGZO Films, Rishabh Kishore, Kavita Vishwakarma, Arnab Datta; Department of Electronics & Communication Engineering, Indian Institute of Technology (IIT) Roorkee

Breakdown characteristics of sputtered IGZO films were assessed employing non-identical annealed fixed thickness IGZO metal-insulator-metal (MIM) capacitors. Highest time to breakdown (t_{BD}) in ozone annealed film was attributed to its reduced intrinsic oxygen vacancies (V_O^I) among the remaining samples which was furthermore corroborated by XPS analysis and slope of the Weibull distribution (β). For a given sample, β was found to remain weakly sensitive to the field and temperature stresses, though it was dependent on the VO^I in IGZO film. Furthermore, XPS correlation was made to assess pivotal role of In-O and Ga-O bonds in IGZO film on governing its critical breakdown field (E_{BD}) and field acceleration factor (Γ)

P25 - Frequency Dependant Gate Oxide TDDB Model, M. Arabi, X. Federspiel, F.Cacho, M. Rafik; Technology R&D, STMicroelectronics, S. Blonkowski, X. Garros; CEA, G. Guibaudo; Univ. Grenoble Alpes

In this work, a new model of the time-dependent dielectric breakdown is proposed as a function of frequency. This is an analytical model based on an experimental observations of gate oxide breakdown at high frequencies on 28nm FDSOI technology in NMOS. This model considers two significant conditions: at first, the defect generation rate in the gate oxide is not constant over time, secondly, the recovery time is negligible. Following the experimental evidences, we found it possible to model four important characteristics of AC breakdown: frequency dependence, voltage acceleration factor (VAF), activation energy Ea, and the change of Weibull slope from DC to AC.

P26 - Robust Off-State TDDB Reliability of n-LDMOS, Wen Liu, Johnatan Kantarovsky; GLOBALFOUNDRIES, Essex Junction, Dimitris P. Ioannou, GLOBALFOUNDRIES, Hopewell Junction, Byoung Min; GLOBALFOUNDRIES, Malta, Tanya Nigam; GLOBALFOUNDRIES, Santa Clara

We report on the gate oxide reliability of n-type LDMOS which is integrated in a 90nm BiCMOS technology and is optimized to offer a robust off-state TDDB reliability performance. In contrast to previous published results, we demonstrate that off-state TDDB lifetimes show very weak dependence on the applied drain bias, Vd, thanks to the carefully optimized NWell drift region that effectively shields the channel from the deleterious high electric fields associated with high Vd operation and significantly reduces the vertical electric field across the gate oxide as shown by TCAD simulation results. TDDB lifetimes are then mainly modulated by the gate voltage and are found to be comparable to the lifetimes obtained under inversion and accumulation modes, hence enabling a reliable operation under high Vdg bias levels.

P27 - Combining SILC and BD Statistics for Low-Voltage Lifetime Projection in HK/MG Stacks, Andrea Vici; ESAT, KU Leuven & imec, Robin Degraeve, João Pedro Bastos, Philippe Roussel ; imec, Ingrid De Wolf; imec & Department Material Science, KU Leuven

We propose a geometrie statistical model to describe stress-induced leakage current (SILC) as a function of trap density (D_{ot}). We demonstrate how soft breakdown measured on smaller devices is controlled by a 2-trap percolation path and how its voltage dependence coincides with the 1 to 2 traps transition of SILC measured on larger devices. Finally, assuming the high-k as the breaking layer, we convert the 1-trap leakage current into D_0t·

P28 - A Realistic Modeling Approach To Explain the Physical Mechanism of TDDB For Automotive

Grade-Zero Applications, C. H. Yang, P. S. Chien, Y. S. Cho, W.S. Hung; More Than Moore Technology Quality & Reliability Division, Taiwan Semiconductor Manufacturing Company

Gate oxide reliability face a big challenge in high temperature automotive application (auto-grade 0). In this paper, we fully discuss the physical mechanism of oxide trap interaction and point out the oxide reliability weakness. It is found the unexpected TDDB behavior at high temperature, include strong SBD, the relationship of voltage acceleration change, and non-linear temperature effect. In addition, the AC/DC effect found more obvious recovery effect. Finally, for mass production, we also import the confidence level usage to give a reasonable lifetime margin for mass production.

P29 - Electric Field Impact on Lateral Charge Diffusivity in Charge Trapping 3D NAND Flash Memory, Juwon Lee, Junho Seo, Jeonghun Nam, YongLae Kim, Ki-Whan Song; Flash PE Team, Jai Hyuk Song; Flash Product & Technology, Samsung Electronics, Woo Young Choi; Department of Electrical and Computer Engineering, Seoul National University

We propose a novel method of predicting electron and hole lateral diffusion in a charge trapping layer (CTL) of 3D TLC NAND, which can estimate the long-term lateral migration (LM) behavior in a short time. By monitoring the threshold voltage change (ΔV_u) of the select cell under various bias and temperature conditions, we observe that electron and hole lateral diffusivity matches well with the Poole-Frenkel (PF) model. The lateral diffusivity is extracted by measuring ΔV_{th} when the electrons and holes of neighboring cells reach the selected cell. by accelerating the diffusivity up to 10.35 times with biasing 3V to neighbor cell, the measurement time required for forecasting the long-term LM becomes 94% shorter with <5.5% error.

P30 - An Abnormal Negative Temperature Dependence of Erase-State Vt Retention Shift in 3-D NAND Flash Memories, Y. H. Liu, Y. S. Yang, T. C. Zhan, W. Lin, A. C. Liu, Y. C. Hsu; Phison Electronics Corp., M. Hu, Z. J. Liu; Guangdong OPPO Mobile Telecommunications Corp., Ltd.

Temperature-accelerated methods are generally used for lifetime evaluations in Flash memories products. However, in this article, an anomalous negative temperature dependence of erase-state threshold voltage (V_t) retention gain in post program/erase (P/E) cycled 3-D NAND Flash memories is reported for the first time, which would lead to a methodological problem of the conventional temperature-accelerated life-test approach. Based on our experiment results, the phenomenon is realized due to the combination of two physical mechanisms. Erase V_t gain at lower temperatures is mainly attributed to silicon nitride (SiN) trapped hole vertical loss via oxide trapped charges created by high P/E cycling stress. At higher bake temperatures, the influence of oxide trapped electron detrapping process is enhanced and V_t gain is therefore reduced. By performing a special experiment, the activation energy of the trapped electron detrapping process is extracted.

P31 - Investigation of Retention Characteristics in a Triple-Level Charge Trap 3D NAND Flash Memory, Yunjie Fan, Zhiqiang Wang, Shengwei Yang, Kun Han, Yi He; Yangtze Memory Technologies Co., Ltd.

In this paper, the long term data retention characteristics consisting of three main charge loss mechanisms, detrap, trap-assisted tunneling (TAT), and lateral migration (LM), are investigated in charge trap (CT) 3D NAND flash memory. Three mechanisms were completely separated through experiment design, and each activation energy *(*E_a) was extracted with Arrhenius model well. The detrap mechanism shows the largest E_a, followed by LM and TAT mechanisms. It is interesting that the contribution rate (CR) of each mechanism is related to time-constant (τ) in the early part of bake time, and depends on the final charge loss in the latter part of bake time. It is inferred that the retention bottleneck is low program level state at high temperature and is high program level state at low temperature. TAT mechanism dominates the final charge loss regardless of temperature region and program level state. In addition, an effective method is proposed to suppress the LM effect.

P32 - High-k MIM Dielectric Reliability Study in 65nm Node, Ravi Achanta, V. McGahay, S. Boffoli; GlobalFoundries, C. Kothandaraman, J. Gambino; onsemi

New multi-layer ALD $HfO_2/Al_2O_3/HfO_2$ laminate film with a capacitance density 8.3 fF/um^2 is evaluated in a MIM capacitor, in 65nm node process, for emerging applications in the automotive space which require higher use voltage and temperature than CMOS logic and DRAM applications. Apart from the typical considerations such as leakage current, capacitance linearity etc. the dielectric relaxation current behavior is also studied. We have performed a thorough reliability study on these films and demonstrate that they meet the stringent requirements for automotive safety applications.

P33 – Withdrawn

P34 – Withdrawn

P35 - Effect of OTS Selector Reliabilities on NVM Crossbar-Based Neuromorphic Training, Wen Ma; Western Digital Research, Brian Hoskins, Matthew W. Daniels, Jabez McClelland; Physical Measurement Laboratory, National Institute of Standards and Technology, Tung Thanh Hoang; Western Digital Research, Yutong Gao, Gina Adam; Electrical and Computer Engineering, George Washington University, Martin Lueker-Boden; Western Digital Research

This paper studies the use of 1-selector-1-resistor (1S1R) devices as the cross-point components in a crossbar array for deep neural network (DNN) training. Two training algorithms—minibatch gradient descent (MBGD) and a low-rank approximation to MBGD—are evaluated with compact models of ovonic threshold switching (OTS) selectors considering several reliability issues, and resistive random-access memory (ReRAM), a type of emerging non-volatile memory (NVM) device. We explore various reliability concerns of the OTS selectors including the low on-state conductance, threshold voltage variation, and internal voltage offset, etc. and propose corresponding techniques to overcome the reliability challenges.

P36 - Combining Measurements and Modeling/Simulations Analysis to Assess Carbon Nanotube Memory Cell Characteristics, J. Farmer, D. Veksler, E. Tang, G. Bersuker; MTD, D. Z. Gao, A.-M. El-Sayed, T. Durrant, A. Shluger; Nanolayers Research Computing LTD, T. Rueckes, L. Cleveland, H. Luan, R. Sen; Nantero Inc.

A simulation package for CNT memory cells is developed, based on computational modeling of both the mesoscopic structure of carbon nanotube films and the electrical conductivity of inter-CNT contacts. The developed package enables the modeling of various electrical measurements and identification of a range of operation conditions delivering desirable device characteristics. This approach opens the path for optimization of the CNT fabric to meet performance requirements.

P37 - Investigation on Contacts Thermal Stability for 3D Sequential Integration, S. J. Mao, J. B. Liu, Y. Wang, W. B. Liu, Y. P. Hu, H. W. Cui, R. Zhang, H. C. Liu, Z. X. Wang, N. Zhou, Y. K. Zhang, H. Yang, Z. H. Wu, Y. L. Li, J. F. Gao, A. Y. Du, J. F. Li; Institute of Microelectronics, Chinese Academy of Sciences, J. Luo, W. W. Wang, H. X. Yin; Institute of Microelectronics, Chinese Academy of Sciences & School of Microelectronics, University of Chinese Academy of Sciences

Contacts stability versus thermal budget is a major concern in 3D sequential integration. We experimentally investigate the thermal stability of n-type contacts on Si and p-type contacts on SiGe in terms of specific contact resistivity (ρ_c). An improved ρ_{cn} performance featuring lower magnitude and better thermal stability has been demonstrated for Ti silicide contacts on n^+-Si with Ge pre-amorphization implantation (PAI). For p-type contacts, it is found that Ni has lost its high work function advantage on p^{++}-SiGe and Ti germanosilicide contacts show ρ_{cp} outperformance. CMOS contact scheme based on single Ti instead of dual Ti and Ni has hence been evidenced to be more suitable for 3D sequential integration.

P38 - Applying Universal Chip Telemetry to Detect Latent Defects and Aging in Advanced Electronics, A. Evelyn Landman; R&D, proteanTecs, 36 Kdoshei Bagdad, Alex Burlak; R&D, proteanTecs, 1200 Route 22 East,

C. Nir Sever, D. Marc Hutner; Business, proteanTecs, 36 Kdoshei Bagdad

Mission critical applications and zero downtime tolerant systems are dominating semiconductor consumption, with AI at the Datacenter, 5G and Automotive being implemented on leading edge FinFET silicon technologies and advanced 2.5D and 3D packaging, required to perform at increasing functionality and performance profiles, for extended lifetime durations. With these advanced technologies, comes a plethora of new concerns to the product health and reliability. Out of these applications, Automotive deserves special consideration being subject to additional regulatory and safety concerns.

This paper will discuss how deep data analytics based on Universal Chip Telemetry™ (UCT) offers a new approach to lifecycle health and performance monitoring in advanced electronics. By combining on-chip monitoring with machine learning inference in the cloud and edge, production quality is improved through advanced latent defect detection, while lifetime reliability is increased through degradation monitoring and predictive fault detection.

P39 - Pre-O2 Treatment for LNA Gate Oxide Leakage Improvement, Zheng Ke, Sachin Goyal, Solomon Arputharaj, Wee Yee Wendy Lau, Tan Tam Lyn, Lim Dau Fatt, Pandurangan Madhavan, Chandrasekar Venkataramani; GLOBALFOUNDRIES Singapore Pte Ltd.

Gate oxide leakage issue is one of key reliability concern as transistor is scaled down. The prominent leakage was observed in SiON based thin gate oxide of LNA which is related to under optimized interface between gate oxide and active silicon. A pre-nitridation O_2 treatment were introduced to significantly suppress the trap assist tunneling behavior and enhanced the gate oxide TDDB performance without degrading the DC electrical and RF performance of the 5G LNA device. This process optimization also benefits the manufacturability in mass production.

P40 - Novel Electrical Detection Method for Random Defects on Peripheral Circuits in NAND Flash Memory, Bu-il Nam, Youngha Choi, Sungki Hong, Ki-Young Dong, Dooyeun Jung, Byoung-Hee Kim, Eunkyoung Kim, Ki-Whan Song; Flash PE Team, Wontaeck Jung, Sang-Won Park, Soon-Yong Lee, Jai Hyuk Song; Flash Product & Technology, Samsung Electronics, Woo Young Choi; Department of Electrical and Computer Engineering, Seoul National University

We propose an electrical detection method for peripheral circuit (PERI) 'open' random defects. This brand new screening methodology detects only PERI defects by independently controlling the supply voltage (V_{DD}) of each circuitry array at low temperature. The proposed method is confirmed based on experimental, simulation, and physical analysis results. Compared with conventional function test items, our proposed method shows >50% error reduction.

P41 - An Analytical Model of Transient Response of MEMS under High-G Shock for Reliability Assessment, Tianfang Peng, Zheng You; Department of Precision Instrument, Tsinghua University & Key Laboratory of Smart Microsystem (Tsinghua University) Ministry of Education

The assessment of the reliability of MEMS under high- g shock has been challenging and primarily relied on experiments. In this paper, we proposed an analytical model that more accurately described the transient response of MEMS under high-g shock than the currently adopted half-sine description of shock load in the industrial testing standards. Furthermore, we proposed a reliability index β to assess the threshold of the shock amplitude that MEMS structures could survive with the vibrating and fading features of the shock considered. The numerical results based on the shock response spectrum (SRS) analysis have shown excellent accuracy of our proposed model of ours. The index β revealed that the reliability of MEMS structure could be significantly lower under a shock of short duration than it under quasi-static acceleration impulse.

P42 - The Optimal Shape of MEMS Beam under High-G Shock Based on a Probabilistic Fracture Model,

Tianfang Peng, Zheng You; Department of Precision Instrument, Tsinghua University & Key Laboratory of Smart Microsystem (Tsinghua University) Ministry of Education

MEMS designed for high-g shock environments tend to sacrifice their structural performance for reliability concerns. The size and shape of the micro-beam are critical for both the performance and reliability of MEMS. This paper proposes an optimization method that can exploit the structural performance of MEMS beams under mechanical overload. First, we proposed a reliability model to quantify the fracture probability of MEMS beam under shock. Secondly, a performance optimization problem was established based on the variable cross-section beam structure. Finally, the optimal shape of four typical types of MEMS beam was obtained numerically. Without sacrificing their reliability under high-g shock, the driving voltage and the structural sensitivity of the beam of optimal shape were improved by 13-49% and 32-79%, which is a practical optimization design by not changing the manufacturing process drastically.

P43 - NBTI Characterization with in Situ Poly Heater, Yu-Hsing Cheng, Michael Cook, Derryl D. J. Allman; Corporate Research and Development, onsemi

Negative bias temperature instability (NBTI) is a critical concern for CMOS reliability and ultra-fast test system for I_D-V_G characterization at the μs time scale is usually needed due to device relaxation. Poly heater structure provides *in situ* temperature changes to allow different temperatures for stress and measurement in NBTI characterization to reduce recovery in measurement. In this paper NBTI characterization for 5V PMOS devices in a 0.18μm smart power technology utilizing poly heater in a standard test system was investigated with good agreement to test results from fast measurement system.

P44 - Withdrawn

P45 - A Deeper Understanding of Well Charging Reliability with Circuit Relevant Test Structures, T L. Tan, C.W. Eng, H. Xu, J.M. Soon, E. Ebard, M. Siddabathula; Quality & Reliability, GlobalFoundries, B.F. Phoong, K.H. Poh, M. Prabhu; Design Enablement, GlobalFoundries, X.-L. Zhao, J.M. Koo, K. Cho, G.-W. Zhang; Technology Development, GlobalFoundries

Antenna rules relating to well charging is becoming an important aspect to consider in design rule checks on the product apart from the conventional antenna to gate ratio design rules. In this paper, we provided a better understanding of the well charging phenomena in technologies with deep N-Well using different layout configuration test structures that are typical of a circuit. A new power law correlation with a well exponent value based on characterized PID gate leakage data is introduced. Moreover, a comparison of well charging design solutions is also presented and validated on the circuit-like test structures.

P46 - Infant Mortality and Wear-Out Failures in Polymer and MnO2 Tantalum Capacitors, Alexander Teverovsky; Jacobs, NASA/GSFC c. 562, Greenbelt

Reliability testing of modern tantalum capacitors shows the presence of both types, infant mortality (IM) and wear-out (WO) failures. To assure reliable operation, the probability of IM failures should be reduced to below the specified level, and the time of WO inception should be greater than the required useful life of the parts at operation conditions. In this work, several types of MnO2 and polymer cathode tantalum capacitors have been tested at highly accelerated conditions to assess voltage acceleration factors, determine adequate burn-in conditions, and assess the useful life. A modified time dependent dielectric breakdown (TDDB) model has been suggested to explain both types of failure, and a physical mechanism of degradation that is based on migration and reactions of oxygen vacancies explains increase of the defect related, IM failures with the level of stress.

P47 - Reliability of Ferroelectric and Antiferroelectric Si:HfO2 Materials in 3D Capacitors by TDDB Studies, A.Viegas, K. Falidas, T. Ali, K. Kühnel, R. Hoffmann, C. Mart, M. Czernohorsky; Fraunhofer Institute

for Photonic Microsystems IPMS, Center Nanoelectronic Technologies (CNT), J. Heitmann; Institute of Applied Physics, Technical University Bergakademie Freiberg

A systematic study of the time-dependent dielectric breakdown of 3D ferroelectric (FE) and antiferroelectric (AFE) Si:HfO_2 capacitors is reported. The voltage and temperature acceleration of characteristic breakdown time is studied. The 10 year lifetime extrapolation is projected to be 2.3 MV/cm and 2.7 MV/cm for 20 nm FE and AFE devices respectively. Further, 10 nm AFE devices had projected lifetime at 2.5 MV/cm at 100 °C. The effect of the polarization measurements on the TDDB is studied and the impact to the lifetime extrapolation was found to be neglectable.

P48 - Nanoscale Analysis of Breakdown Induced Crack Propagation in DTSCR Devices, Xinqian Chen, Zuoyuan Dong, Chaolun Wang, Fang Liang, Xing Wu; Key Laboratory of Multidimensional Information Processing, School of Communication and Electronic Engineering, East China Normal University, Yuxin Zhang, Feibo Du, Zhiwei Liu; Center for Advanced Semiconductor & Integrated Micro-System, University of Electronic Science and Technology of China, Fei Hou ; School of Electronic Information and Electrical Engineering

In the advanced technology process, owing to the low and tunable trigger voltage, diode-triggered SCRs (DTSCRs) are widely used in low-voltage applications with extremely narrow electrostatic discharge (ESD) design margins. The breakdown of DTSCRs ESD structure with abnormal leakage current under transmission line pulsing stressing was studied in this work. The physical origins of DTSCRs have been established through failure analysis (FA). The mismatch of the thermal expansion coefficient of local materials results in redundant stress. Such redundant stress induce the structure dislocations and cracks were captured by transmission electron microscopy at atomic scale. A multi-physical simulation is conducted to scrutinize the breakdown transient process.

P49 - Insights on Inter-Metal Reliability Assessment of High Voltage Interconnects, Kwang Sing Yew, Ran Xing Ong, Hin Kiong Yap, Wanbing Yi, Jacquelyn Phang, R. Chockalingam, Juan Boon Tan, GLOBALFOUNDRIES, 60 Woodlands Industrial Park D St 2

Reliability qualification of HV interconnects is more complicated due to the additional inter-metal impact under high voltage operation. Typically, this is less critical under nominal voltage operation. Unlike intra-metal structure, the film stack, and the bottom physical profile of the inter-metal structure are uneven. This explains the reliability response showing the dependence on metal line width and bias polarity. We show that the E-field distribution is not uniform, with the highest E-field density observed at the bottom corners of the metal line. This corresponds to the uneven bottom metal profile with sharp corners. Hence, for a complete inter-metal TDDB reliability qualification, the impacts from test structure design, process variation, and testing methodology need to be considered.

P50 - Degradation Behaviors of 22 nm FDSOI CMOS Inverter under GHz AC Stress, Yaru Ding, Wei Liu, Yiming Qu, Liang Zhao; College of Electronic Engineering and Information Science, Zhejiang University & International Joint Innovation Center, Zhejiang University, Yi Zhao; College of Electronic Engineering and Information Science, Zhejiang University & International Joint Innovation Center, Zhejiang University & State Key Laboratory of Silicon Materials, Zhejiang University

In this work, Gigahertz (GHz) AC signals are stressed at the input terminal of 22 nm FDSOI inverters and the degradation behaviors of transistors in the inverter are found to be different from that under the single device stress. These transistors work under different bias schemes compared to the regular single device measurements, where the AC stress is applied at the gate and DC stress is applied at the drain. To more precisely characterize the transistor reliability in logic circuits, we design the layout to measure the actual degradation of transistors in the inverter directly. The noise margin of the inverter and SRAM cell comprised of this inverter is also studied. The results in this study show that, in a real inverter, the degradation of pMOSFET is overestimated if the BTI result of single device is used.

P51 - Deep Level Effects and Degradation of 0.15 um RF AlGaN/GaN HEMTs with Mono-Layer and Bi-Layer AlGaN Backbarrier, Z. Gao, F. Chiocchetta, C. De Santi, N. Modolo, F. Rampazzo, M. Meneghini, G. Meneghesso, E. Zanoni; Dipartimento di Ingegneria dell'Informazione, Università di Padova, H. Blanck, H. Stieglauer, D. Sommer, L. Benoit, J. Grünenpütt, Jr-Tai. Chen; United Monolithic Semiconductors GmbH, Wilhelm-Runge-Strasse 11, D-89081 Ulm, O. Kordina, J-C Jacquet, C. Lacam, S. Piotrowicz; III-V Lab, Av. Augustin Fresnel, 91767 Palaiseau

Deep level effects and on-wafer reliability have been evaluated in 0.15 μm AlGaN/GaN HEMTs differing for buffer compensation (C or Fe) and for epitaxial structure (C-doped monolayer devices with only C-doped region; C-doped bilayer samples with a barrier between the channel and the C-doped region). In monolayer devices trapping effects lead to the presence of a long time constant (50s) in drain current transients, related to the presence of C_N defects; interaction with deep levels in C-doped buffer leads to knee voltage walkout, R_{ON} increase and recoverable IDS degradation. Negative trapped charge in the gatedrain region reduces the electric field with respect to bilayer devices. Results from semi-on and on-state step stress show that by using a 'Bi-layer' AlGaN barrier, the interaction between C-related deep levels and channel hot electrons can be effectively reduced, thus alleviating trapping effects and parametric degradation, and giving the opportunity of fully exploiting the improved confinement offered by the C-doped buffer, at the expenses of a tolerable decrease of breakdown voltage.

P52 - Correlated Effects of Radiation and Hot Carrier Degradation on the Performance of LDMOS Transistors, Bikram Kishore Mahajan, Yen-Pu Chen, Muhammad Ashraful Alam; Elmore Family School of Electrical and Computer Engineering, Purdue University, Ulisses Alberto Heredia Rivera, Rahim Rahimi; School of Materials Engineering, Purdue University

Over the past few decades, power electronics devices have found numerous applications, including high energy physics, drones, space electronics, etc. It is well-known that the devices used in these applications are often subjected to a high dose of radiation, and unlike traditional applications, it is not possible to frequently replace these power FETs (e.g., LDMOS). Therefore, it is essential to accurately predict the long-term integrated degradation of these power FETs in the presence of radiation. In this paper, we: (a) expose LDMOS transistors to various Total Ionizing Dose (TID) of gamma radiation and characterize the degradation in terms of threshold voltage shift (ΔV_{TH}), subthreshold slope (ΔSS); (b) quantify the dose-dependent generation of interface traps (ΔN_{IT}) and trapped charges (ΔN_{OT}) using a novel charge pumping technique; (c) introduce hot carrier degradation (HCD) models to explore the physical origin of the defects and their correlation with TID; and (d) establish the universality of the degradation kinetics and illustrate that the model and inferences drawn from the findings in this paper can be applied to other LDMOS devices as well. This analysis takes us a step closer towards a generalized TID-HCD model for power FETs that incorporates all sources of variation (electrical, thermal, and radiation) during device operations.

P53 - Accelerator-Based Thermal-Neutron Beam by Compact and Low-Cost Moderator for Soft-Error Evaluation in Semiconductor Devices, Taiki Uemura, Byungjin Chung, Jegon Kim, Hyewon Shim, Shinyoung Chung, Brandon Lee; Samsung Foundry, Samsung Electronics, Co., Ltd., Jaehee Choi; Semiconductor Research and Development Center, Samsung Electronics, Shota Ohnishi, Ken Machida; Samsung R&D Institute Japan

This paper proposes an accelerator-based neutron beam to evaluate thermal-neutron-induced soft-error rate (tnSER) in semiconductor devices. The thermal-neutron flux is sufficient for the tnSER evaluation in the beam, and the moderator for the beam is compact, and we can perform the tnSER test at many facilities. We have evaluated tnSER in an SRAM with the proposed beam and a nuclear reactor, and the tnSER is in good agreement between the tests with the proposed neutron beam and the nuclear reactor.

P54 - Design and Heavy-Ion Testing of MTJ/CMOS Hybrid LSIs for Space-Grade Soft-Error Reliability, K. Watanabe, T. Shimada, K. Hirose, H. Shindo, D. Kobayashi; Japan Aerospace Exploration Agency, Tsukuba, T. Tanigawa, S. Ikeda, T. Shinada, H. Koike, T. Endoh; Tohoku University, Sendai, T. Makino, T. Ohshima; National Institutes for Quantum Science and Technology

We show our attempt to design space-grade low-power CMOS LSIs enhanced by magnetic tunnel junctions (MTJs). The validity is discussed by using high-energy heavy-ion experiments and macrospin simulations combined with single-event transient noise current modeling. Possible latent damage induced by heavy ions are also explored.

P55 - Modeling Time and Bias Dependence of Classical HCD Mechanism (Peak ISUB Stress) in n-MOSFETs, Himanshu Diwakar, Karansingh Thakor, Souvik Mahapatra; Department of Electrical Engineering, Indian Institute of Technology Bombay

Time and drain bias dependence of HCD under peak I_{SUB} ($V_G \sim V_D/2$) stress are modeled. Published n-MOSFET data for different L_{CH} (2-0μm to 37nm), T_{OX} (35nm to 1.85nm), type of junction (HDD, LDD/HDD, SDE/HDD) and stress V_D (8V to 1.6V) are analyzed. A compact model is used to model the time kinetics and to explain its difference *(i.e.,* power law or non-power law) in devices having different types of junctions. The dominant energy model is used for V_D dependence, and the model parameters are obtained with scaling. The time kinetics and V_D dependence are also modeled using TCAD simulations.

P56 - Decoupling of NBTI and Pure HCD Contributions in p-GAA SNS FETs under Mixed VG/VD Stress, Nilotpal Choudhury, Ayush Ranjan, Souvik Mahapatra; Department of Electrical Engineering, Indian Institute of Technology Bombay

Ultrafast measurements (with 10μs delay) are done to characterize the Negative Bias Temperature Instability (NBTI) and Hot Carrier Degradation (HCD) induced threshold voltage shift (Δv_T) in p-channel Gate All Around Stacked Nano-Sheet (GAA-SNS) Field Effect Transistors (FETs). A model framework is proposed to estimate the measured $\Delta v\tau$ time kinetics during and after NBTI and HCD stress. The BTI Analysis Tool (BAT) framework is calibrated using pure NBTI data (drain bias, V_D, at 0V) across gate bias (V_G) and temperature (T) and is subsequently used to estimate the underlying NBTI contribution during and after HCD stress under full V_G/V_D space in the presence of Self-Heating (SH) effect. The pure HCD kinetics is calculated using an empirical model, with V_G, V_D and T dependence incorporated via a vertical field enhanced dominant energy model.

P57 - Optimized LDMOS Offering for Power Management and RF Applications, S. Cimino, J. Singh, J. B. Johnson, W. Zheng, Y. Chen, W. Liu, P. Srinivasan, O. Gonzales, M. Hauser, M. Koskinen, K. Nagahiro, Y. Liu, B. Min, T. Nigam; GLOBALFOUNDRIES US Inc, 400 Stone Break Road Extension, N. Squib; Rensselaer Polytechnic Institute

The suitability of a 12nm FinFET LDMOS offering toward a broad range of applications has been demonstrated. This work focuses on key reliability aspects with respect to usage conditions typical of RF applications. A detailed overview of the impact of well-known degradation mechanisms, such as conductive and non-conductive Hot Carrier Injection and the off-state Time Dependent Dielectric Breakdown is presented. The conflicting requirements of long-life reliability and high time zero performance can be resolved through process and/or design optimization.

P58 - Reverse Body Bias Dependence of HCI Reliability in Advanced FinFET, Md Iqbal Mahmud, Rakesh Ranjan, Ki-Don Lee, Pavitra Ramadevi Perepa, Caleb Dongkyun Kwon; Samsung Austin Semiconductor, LLC, 12100 Samsung Blvd, Austin, Seungjin Choo, Kihyun Choi; Samsung Foundry Business, Samsung Electronics

The effect of reverse body bias on hot carrier (HCI) reliability is studied in details at CHE (channel hot carrier) and DAHC (drain avalanche hot carrier) stress conditions in advanced standard gate n-channel FinFET transistors. HCI degradation is found to be independent of reverse body bias, when the body bias, Vb is low (0V ~ -1V). However, HCI starts to aggravate at further negative Vb (-1V ~ -2V) for both CHE and DAHC conditions, showing strong dependence on the transverse electric field. The physical mechanism is attributed to the increased e-h pair generations, enhancing electron trapping in the gate oxide. This study addresses a key reliability constraint for circuit designers while designing tuned body bias circuitry.

P59 - Impact of Electrical Defects Located at Transistor Periphery on Analog and RTN Device Performance, L. Pirro, P. Liebscher, C. Brantz, M. Kessler, H. Herzog, O. Zimmerhackl, R. Jain E. Ebrand, K. Gebauer, M. Otto, A. Zaka, J. Hoentschel ; GlobalFoundries Fab 1 LLC & Co.KG

In this work, analog and RTN performance of transistors operating in low current conditions were reported. In subthreshold regime the RTN signal is driven by defects located at the STI edges. Experimental data show that reducing the amount of electrical impurities present at the device periphery, lead to RTN improvement without changing neither the transistor targeting nor its reliability. Furthermore, the transistor noise sensitivity to temperature and body bias are decreased. Empirical correlation between RTN and intrinsic gain is also discussed, which can be employed for fast inline process monitoring of defects present at the STI edges.

P60 - SiGe Gate-All-around Nanosheet Reliability, Huimei Zhou, Miaomiao Wang, Ruqiang Bao, Curtis Durfee, Liqiao Qin, Jingyun Zhang; IBM Research Division, Albany Nanotech

In this paper, we present a detailed study of negative bias temperature instability (NBTI) and Time dependent dielectric breakdown (TDDB) reliability in p-type stacked gate-all -around (GAA) Nanosheet (NS) transistors with SiGe channel and compared with NS Si pFETs. Robust NBTI and TDDB reliability performance is achieved on SiGe gate-all-around NS.

P61 - Failure Analysis Addressing Method of Optically Undetected Defectivity on 4H-SiC PowerMOSFET Epitaxial Layer, S. Alessandrino, B. Carbone, F. Cordiano, B. Mazza, A. Russo, W. Coco, M. Boscaglia, A. Di Salvo, A. Lombardo, D. Scarcella, E. Vitanza; STMicroelectronics, Stradale Primosole, P. Fiorenza; Consiglio Nazionale delle Ricerche-Istituto per la Microelettronica e Microsistemi (CNR-IMM)

The issues related to the failure analysis of 4H-SiC PowerMOSFET failed at EWS (Electrical Wafer Sorting) such as the channel leakage current is investigated. In particular, EWS is carried out in the namely defect free wafers areas monitored at several inline levels. This paper reports on the electrical based methods used to spot macroscopic defects even if they are invisible at optical wafer inspections. In particular, the current separation technique on source and gate terminals allowed to reduce the number of candidate samples to be investigated during failure analysis increasing the whole analysis success rate.

P62 - Static Performance and Reliability of 4H-SiC Diodes with P+ Regions Formed by Various Profiles and Temperatures, Stephen A. Mancini, Seung Yup Jang, Dongyoung Kim, Justin Lynch, Woongje Sung; State University of New York Polytechnic Institute, College of Nanoscale Science and Engineering, Zeyu Chen, Yafei Liu, Yafei Liu, Balaji Raghothamachar, Michael Dudley; Department of Material Science and Chemical Engineering, Stony Brook University, Minseok Kang, Anant Agarwal; Department of Electrical and Computer Engineering, The Ohio State University, Nadeemullah Mahadik, Robert Stahlbush; Naval Research Laboratory, Washington DC

Several designs of 1.2kV-rated 4H-SiC PiN diodes and Junction Barrier Schottky (JBS) diodes have been successfully fabricated with various P+ implantation conditions resulting in different junction profiles. P+ regions were implanted at both room temperature and elevated temperature (600°C) to monitor the generation of Basal Plane Dislocations (BPDs) and study their impact on device long term reliability. It was found that, when the dose in the deeper portion of the junction (implemented by high energy implantations) is well suppressed, static and long-term reliability performances of room temperature implanted devices can be maintained similar to those of high temperature implanted devices.

P63 - Influence of SiC Epitaxial Wafer Quality on Yield of 1.2kV SiC-DMOSFETs, Junji Senzaki, Ryoji Kosugi, Keiko Masumoto, Takeshi Mitani, Takeharu Kuroiwa, Hiroshi Yamaguchi; Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Technology

This work presents the influence of SiC epitaxial wafer quality on yield of 1.2kV SiC-DMOSFETs. Various wafer

quality indicators were estimated by an integrated wafer quality evaluation system. SiC-DMOSFETs were fabricated on six 100 mm 4H-SiC epitaxial wafers. We show that the yield of SiC-DMOSFETs is related to threading screw dislocation density, defect density and bunched-steps length density evaluated by an integrated wafer quality evaluation system. A one-to-one analysis of multiple inspection data for SiC epitaxial defects and wafer-level electrical test results reveals the main factors in the yield of SiC-MOSFETs.

P64 - Characteristic Degradation of Power MOSFETs by X-Ray Irradiation and their Recovery, Masato Shiozaki, Takashi Sato; Graduate School of Informatics, Kyoto University

Power device characteristics are affected by X-rays used during the inspection of power modules. In this study, the effects of materials and structures of power MOSFETs on the overall degradation were analyzed by irradiating Si MOSFETs and SiC MOSFETs with X-rays using a commercial inspection system. In addition, the effectiveness of thermal and gate voltage annealing was investigated for the irradiated devices. The experimental results confirmed the high radiation tolerance of SiC MOSFETs. In addition, the irradiated devices exhibited difficulty in recovering the shifted threshold voltage without compromising the reliability of the device, indicating that the effects of degradation persisted for a long time.

P65 - Defects in 4H-SiC Epilayers Affecting Device Yield and Reliability, Robert Stahlbush, Nadeemullah Mahadik; Naval Research Laboratory, Peter Bonanno; Naval Research Laboratory, former post-doctoral fellow, Jake Soto, Bruce Odekirk; Microchip Technology Inc., Bend, Woongje Sung; SUNY Polytechnic Institute, Albany, Anant Agarwal; The Ohio State University, Columbus

Forty nine silicon carbide 150 mm wafers from three commercial vendors to be used for fabricating MOSFETs were examined by UVPL imaging to count their concentration of basal plane dislocations, inclusions, micropipes and trapezoids. The wafers were from three vendors, and wafers with 10 um, 30 um and 60 um epitaxial layers were evaluated. The wafers with 10 um and 30 um epilayers were virtually free of BPDs, while BPD concentrations of the wafers with 60 um were too high for commercial use. Concentrations of inclusions, micropipes and trapezoids were also evaluated. Most of the wafers had acceptable levels of these defects, but device yield would be improved by more consistently having low concentrations.

P66 - Characterization of Electron Traps in Gate Oxide of SiC MOS Capacitors, Yutaka Terao; Fuji Electric Co., Ltd., Takuji Hosoi; School of Engineering, Kwansei Gakuin University, Shinya Takashima; Fuji Electric Co., Ltd., Takuma Kobayashi, Takayoshi Shimura, Heiji Watanabe; Graduate School of Engineering, Osaka University.

The electron trapping in gate oxides of SiC-MOS capacitors were studied by electron injection. The trapped electron densities calculated using the flat-band voltage shift were analyzed.There are possibly three types of electron traps with different capture cross sections. The oxide grown by LPCVD has slightly lower electron trap density than the oxides by thermal oxidation or TEOS-PECVD. The obtained trapped electron densities were found to be one order of magnitude higher than that of Si-MOS and there may be large room for improvement of the electron trap in the gate oxide of SiC-MOSFET for better VT reliability.

Thursday, March 31

Keynote 4
Thursday, March 31, 08:00 a.m. – 08:45 a.m. CDT
Venue: International III & IV

KN4 (Keynote) - New Reliability Ecosystem: Maximize Technology Value to Serve Diverse Markets, Pei-Jean Liao; TSMC, Jun He; Quality and Reliability, Taiwan Semiconductor Manufacturing Company, Ltd.

In past decades, continuous technology advancement has been accelerating semiconductor evolution to enrich our daily life. Today, advanced logic technologies are the key drivers for Mobile and HPC segments. Incorporating additional specialty technologies (HV, RF, Non-Volatile Memory, MEMS, CIS, etc.) empowers new applications. It also enable further customization of process and designs that is essential to fulfill different product needs. However, the past standardized methodologies with logic based bias and failure criterion fall short of enlarging technology envelope on top of meeting field expectation. Therefore, TSMC has been developing a circuit-based qualification approach offering accurate assessment on reliability lifetime to direct device offering and customizing process for specific product usage. A comprehensive reliability platform covering from design stage to mass production has been deployed for different applications which will be a general practice for future technologies. Along the way, we have been establishing our partnership across IP providers, circuit and system designers as well as reliability communities to have joint development by DFR (design for reliability) and DFT (design for testing). This new ecosystem on reliability incorporated DTCO (Design-Technology Co-optimization) is the next key focus to unleash more innovations and maximize process technology value with fast time-to-market.

Break
Thursday, March 31, 08:45 a.m. – 09:05 a.m. CDT

9A – Intro
Thursday, March 31, 09:05 a.m. – 09:10 a.m. CDT

9A - PR (Product Reliability)
Thursday, March 31, 09:10 a.m. – 10:25 a.m. CDT
Venue: International I & II

09:10 a.m.
9A.1 (Invited) - West Coast Wildfire Impact Assessment on Si Photonics Optical Transceiver Pluggable Module Assembly and Performance, Quan Tran, Ronald Gayhardt, Tin Nguyen, Arif Zaman; Silicon Photonic Product Division/ Intel Corporation

The recent natural wildfires on the US west coast generated airborne particles that stayed suspended in the atmosphere for days or weeks before precipitating onto the ground. Many of those particles were able to pass through the HVAC systems of various buildings and redeposit on equipment and devices inside these buildings. Among such devices, optical transceivers could have their performance degraded or fail due to the particles accumulating in their optical paths, which may include lenses and other opto-mechanical components. While existing standards provide susceptibility risk assessments to fine dust particles (GR-326-CORE Issue 4, Sec. 4.4.4.1 Dust Test & Sec. 5.3.7 Dust Test), corrosive gases (GR-1217-CORE Issue 1, Sec. 7.3.4 Mixed Flowing Gas Testing & 9.1.3 Four Gas MFG Testing), smoke and fire (Ref. ASTM E1678), we were not aware of an existing standard covering how to evaluate the impact of wildfire by-products on optical transceiver reliability. This paper documents our approach to evaluate the optical transceivers' susceptibility to failure due to wildfire airborne particles.

09:35 a.m.
9A.2 - Degradation Mechanisms in Germanium Electro-Absorption Modulators, Artemisia Tsiara, Alicja Lesniewska, Philippe Roussel, Srinivasan Ashwyn Srinivasan, Mathias Berciano, Marko Simicic, Marianna Pantouvaki, Joris Van Campenhout, Kristof Croes, IMEC, Kapeldreef 75, 3001 Leuven

Reliability analysis on Ge Electro-Absorption Modulators suggest that different physical mechanisms are involved in the dark current degradation during electrical stress. An "incubation time" followed by a power-law dependent dark current increase suggests the filling of pre-existing defects and the creation of traps at the Ge/Si and Ge/Ox interface. Even though the dark current degrades during reliability testing, actual failures are not expected to happen at nominal operation conditions and times. Finally, performance evaluation after more than

4000h of electrical stress, reveals no degradation of the electro-optical parameters.

10:00 a.m.
9A.3 - Wafer-Level Aging of InGaAs/GaAs Nano-Ridge p-i-n Diodes Monolithically Integrated on Silicon, Ping-Yi Hsieh, Ingrid De Wolf; Dept. Materials Science, KU Leuven, Kasteelpark Arenberg 10, 3001 Leuven & IMEC, Kapeldreef 75, 3001 Leuven, Artemisia Tsiara, Barry O'Sullivan, Didit Yudistira, Marina Baryshnikova, Bernardette Kunert, Marianna Pantouvaki, Joris Van Campenhout; IMEC, Kapeldreef 75, 3001 Leuven, Guido Groeseneken; IMEC, Kapeldreef 75, 3001 Leuven & Dept. Electrical Engineering, KU Leuven, Kasteelpark Arenberg 10, 3001 Leuven

For the first time, a reliability study on degradation of InGaAs/GaAs nano-ridge p-i-n diodes monolithically integrated on Si by nano-ridge engineering (NRE) is reported. Wafer-level constant current stress in forward bias shows a gradual power law aging of both forward and dark current. Current crowding and Joule heating near the p-contact are responsible for the degradation in forward bias region. Indications of defect formation and Ti diffusion at the metal/GaAs interface are witnessed. The electrical stress-induced leakage current builds up at reverse bias region, pointing to the degradation of crystal quality. A sintering process lowers the p- contact resistance and improves electrical stability. The high aspect-ratio of the trenches leads to effective threading dislocation trapping: no dislocations have been observed to penetrate the active region during the 5000s stress time. This early work sheds light on realizing electrically robust GaAs diodes on Si and reliable monolithic lasers.

9A - Authors' Corner
Thursday, March 31, 10:25 a.m. – 10:45 a.m. CDT

9B – Intro
Thursday, March 31, 09:05 a.m. – 09:10 a.m. CDT

9B - RT (Reliability Testing)
Thursday, March 31, 09:10 a.m. – 10:25 a.m. CDT
Venue: International III & IV

09:35 a.m.
9B.1 - Method to Evaluate Off-State Breakdown in Scaled Tri-Gate Technologies, D. Nminibapiel, K. Joshi, R. Ramamurthy, L. Pantisano, I. Meric, S. Ramey; Intel Corporation, 2501 NE Century Blvd, Hillsboro, OR 97124

The source-drain punch-through current in off-state TDDB stress (OSS) is shown to significantly affect off-state breakdown behavior. This paper introduces a modified methodology for conducting OSS in scaled tri-gate devices at accelerated conditions that avoids artifacts associated with punch-through while enabling reliability risk assessment. The methodology is validated for both NMOS & PMOS devices and provides consistent degradation mechanism. Finally, it is shown that on-state gate-oxide TDDB remains the reliability limiter compared to OSS TDDB.

09:10 a.m.
9B.2 - Revealing Stresses for Plasma Induced Damage Detection in Thick Oxides, Daniel Beckmeier, Jifa Hao, Jake Choi, Matt Ring; Intrinsic Reliability, onsemi, South Portland

For the plasma process induced damage (PID) qualification of fabrication processes, stresses are necessary to detect lifetime reduction risks. JEDEC JEP001 requires Hot Carrier Stress (HCS), Bias Temperature Stress (BTS), Time Dependent Dielectric Breakdown (TDDB) stresses, or a revealing stress for this detection. Due to the large number of devices that should be tested in a comprehensive process qualification, the quickly applied revealing stress is preferable. This paper reviews the two main options for the revealing stress for thick oxides: a constant gate current (CGC) and a constant gate voltage (CGV) stress. Our results show that CGC stresses are preferable due to the high robustness exhibited with respect to natural process variation, such as gate oxide thickness

variation among qualification lots or wafers.

10:00 a.m.
9B.3 - Q&R On-Chip (QROC): A Unified, Oven-Less and Scalable Circuit Reliability Platform, Ketul B. Sutaria, Minki Cho, Anisur Rahman, Jihan Standfest, Rahul Sharma, Swaroop Namalapuri, Shiv Gupta, Bahar Ajdari, Ricardo Ascazubi, Balkaran Gill; Q&R Test Chips Design & Data, *TD Q&R, Intel Corporation, Hillsboro

Technology scaling, aggressive operating conditions and shrinking margins caused the emergence of circuit/IP performance aging modelling as an active area of reliability research. Digital, analog and mixed signal circuits experience a broad range of operating conditions, and are subject to various voltage, area, and temperature acceleration factors depending on reliability mechanism, which all stack up to make circuit lifetime prediction a formidable task. In this context, a large volume of circuit-level data, covering statistical process variation and subjected to long-term stress that minimize overstress artifacts, is crucial for effective decision making. To address these challenges, we present "Q&R on Chip" (QROC) -a unified, oven-less and scalable platform for circuit reliability evaluation. With the goal to bridge gaps across design hierarchy from technology building blocks e.g., transistor reliability at one end, to a complex product on the other extreme, we implemented QROC chips with state-of-the-art circuit test structures to evaluate various reliability mechanisms such as transistor aging, dielectric breakdown and thermal stability. Finally, a new stress platform with an on-board FPGA, PC interface and heater socket for temperature control is designed. In this work we present preliminary aging stress data from more than 15000 instances of ring-oscillators (RO) representing 107 unique standard cells, layout styles and device types.

9B - Authors' Corner
Thursday, March 31, 10:25 a.m. – 10:45 a.m. CDT

9C – Intro
Thursday, March 31, 09:05 a.m. – 09:10 a.m. CDT

9C - NC (Neuromorphic Computing Reliability)
Thursday, March 31, 09:10 a.m. – 10:25 a.m. CDT
Venue: Cap Rock I, II & III

09:10 a.m.
9C.1 (Invited) - Monolithic 3D Integration of Oxide Semiconductor FETs and Memory Devices for AI Acceleration, Masaharu Kobayashi; System Design Center *(d.lab),* School of Engineering, The University of Tokyo, Tokyo

IoT edge devices are expected to have high-capacity and low-power storage memory, as well as smart data processing capability such as machine learning and AI, to fully utilize big-data by co-working with cloud computing system. Such edge intelligence requires energy-efficient data movement and computation, which opens new challenges and opportunities to integrated devices, circuits and systems. In this paper, we introduce monolithic 3D integration technologies of (1) high- density embedded memory and (2) in-memory computing, both of which are enabled by oxide semiconductor FETs and memory devices, for AI acceleration. We address key reliability issues regarding manufacturability for each technology.

09:35 a.m.
9C.2 - Suppressing Channel Percolation in Ferroelectric FET for Reliable Neuromorphic Applications, Kai Ni, Zijian Zhao, Shan Deng; Rochester Institute of Technology, Om Prakash; Karlsruhe Institute of Technology; Simon Thomann, Hussam Amrouch; University of Stuttgart, Semiconductor Test and Reliability (STAR)

Channel percolation in ferroelectric FET (FeFET) due to random spatial distribution of switched domains reduces the number of accessible threshold voltage (V_{TH}) states, thus posing a profound reliability challenge when it

comes to its usage as synaptic weight cell in neuromorphic applications. However, channel percolation is not universally present in FeFET and only exists when the channel regions underneath the domains have negligible interaction, e.g., when the domain is large enough. In this work, we performed a comprehensive evaluation on the parameters that could impact neighbor interaction, and hence channel percolation. We reveal that: i) weak gate control with thick ferroelectric (FE) layer enhances neighbor interaction and suppresses channel percolation; ii) higher temperature can also reduce percolation by weakening the gate control. These insights provide an important guideline for to engineer more reliable FeFET analog states.

10:00 a.m.
9C.3 - Ferroelectric FET Threshold Voltage Optimization for Reliable In-Memory Computing, Om Prakash; Karlsruhe Institute of Technology, Kai Ni ; Rochester Institute of Technology, Hussam Amrouch; Chair of Semiconductor Test and Reliability (STAR), University of Stuttgart

Ferroelectric FET (FeFET) emerges as a highly promising candidate for in-memory computing due to its outstanding performance, superior energy efficiency and great scalability. For FeFET, generally the memory window, i.e., the separation between the two threshold voltage (V_{TH}) states, is of interest. The absolute value of the low-V_{TH} and high-V_{TH} states are generally not scrutinized. However, in this work, we demonstrate that a proper engineering of V_{TH} is necessary to ensure correct array operation for in-memory computing applications. We highlight that for all the current-based operations, it is necessary to keep both the V_{TH} states positive to cut off the leakage for grounded unselected cells. To reach that design target, we systematically evaluate various design options for V_{TH} engineering, including the gate metal work function, the body bias, and the buried oxide thickness, in a fully-depleted silicon- on-insulator (FDSOI) FeFET using calibrated TCAD simulations. We establish the design guidelines for V_{TH} engineering to ensure successful operation of in-memory computing applications.

9C - Authors' Corner
Thursday, March 31, 10:25 a.m. – 10:45 a.m. CDT

10A – Intro
Thursday, March 31, 10:45 a.m. – 10:50 a.m. CDT

10A - TX (Transistors)
Thursday, March 31, 10:50 a.m. – 12:30 p.m. CDT
Venue: International I & II

10:50 a.m.
10A.1 - Temperature Dependent Mismatch and Variability in a Cryo-CMOS Array with 30k Transistors, A. Grill, v. John, imec, Kapeldreef 75, 3001 Leuven, J. Michl, B. Parvais, T. Grasser; Institute for Microelectronics, TU Wien, A. Beckers, B. Kaczer, E. Bury, B. Govorean, A. Vaisman Chasin; imec, Kapeldreef 75, 3001 Leuven, S. Tyaginov; imec, Kapeldreef 75, 3001 Leuven & Institute for Microelectronics, TU Wien, M. Waltl; Dep. of Electronics and Informatics, Vrije Universiteit Brussel, Pleinlaan 2, 1050 Brussel & Christian Doppler Laboratory for Single-Defect Spectroscopy in Semiconductor Devices

Integrating CMOS circuits and qubits at cryogenic temperatures is one of the key challenges to mitigate wiring constraints and ensure signal integrity to enable up-scaling of quantum computers. While operating in the GHz-regime, interfaces between classical and quantum circuits need to maintain ultra-low power consumption together with very low noise figures. One approach to reduce power consumption is to optimize designs towards operation at lower supply voltages. However, this reduces the tolerable margins on variability and device to device variations. In this study, we present the time-zero variability and mismatch of thousands of nMOS transistors measured from room temperature down to 4 K. We investigate the physical origins of subthreshold variations at cryogenic temperatures and discuss the correlations between transistor parameters. We estimate the influence of different sources on the on-current variability and observe that another source of mismatch, most likely contact

resistance, is becoming more important at low temperatures.

11:15 a.m.
10A.2 - A Critical Examination of the TCAD Modeling of Hot Carrier Degradation for LDMOS Transistors, Bikram Kishore Mahajan, Yen-Pu Chen, Muhammad Ashraful Alam; Elmore Family School of Electrical and Computer Engineering, Purdue University, Dhanoop Varghese, Srikanth Krishnan, Vijay Reddy; Texas Instruments Inc. Dallas

LDMOS is one of the most widely used power transistors and has a variety of applications across multiple sectors (automobile, photovoltaics, communication, etc.). Unfortunately, the high applied bias makes Hot Carrier Degradation (HCD) a persistent reliability concern for LDMOS transistors. HCD occurs due to the generation of interface defects (N_{IT}) by energetic electrons/holes, and the degradation rate depends sensitively on gate/drain voltages, doping, and transistor geometry. Several efforts have been made to model HCD in TCAD to predict the HCD susceptibility of next-generation LDMOS transistors. However, the lack of characterization techniques to extract $N_{IT}(x)$ in LDMOS makes it difficult to cross-check $AN_{IT}(x)$ obtained from the TCAD models, thereby making reliability-aware predictive design difficult. In this paper, we: (a) determine the physical mechanism of HCD in a planar LDMOS using TCAD; (b) demonstrate the capability of the Super Single Pulse Charge Pumping (S^2PCP) technique to extract $N_{IT}(x)$ at various points in the LDMOS, (c) quantify the spatial and temporal evolution of $N_{IT}(x, í)$, and compare the experimental results with TCAD predictions; (d) identify the key differences between the experimental and TCAD approach and suggest possible physical mechanisms responsible. This analysis establishes the robustness and identifies the limitations of TCAD modeling of HCD in LDMOS devices.

11:40 a.m.
10A.3 - Significant Enhancement of HCD and TDDB in CMOS FETs by Mechanical Stress, Kookjin Lee, Anastasiia Kruv, Ingrid De Wolf; Department of Materials Science, KU Leuven, 3001 Leuven & imec, 3001 Leuven, Ben Kaczer, Mario Gonzalez, Geert Eneman, Oguzhan Orkut Okudur, Alexander Grill, Jacopo Franco, Andrea Vici, Robin Degraeve; imec, 3001 Leuven

Significant enhancement of hot-carrier degradation and time-dependent dielectric breakdown by mechanical stress was observed in CMOS FETs. Mechanical stress was induced locally in the channels of p- and n-type FETs by applying a vertical load with a diamond tip of a nanoindenter. The induced GPa level stress was calculated with finite element modeling. Mechanical stress induces a piezoresistance effect in both p- and n-channels, leading to an increase in source/drain leakage and drive currents and drastic enhancement of impact ionization. This in turn results in strongly enhanced hot-carrier degradation and hot-electron-induced punch-through effects in pFETs and enhanced hot-carrier degradation and time-dependent dielectric breakdown in nFETs.

12:05 p.m.
10A.4 (Late News) - Quantum Mechanical Connection of Schottky Emission Process and its Implications on Breakdown Methodology and Conduction Modeling for BEOL Low-k Dielectrics, Ernest Wu, Baozhen Li; IBM System Group, Essex Junction, Vermont

Using a full quantum mechanical calculation, we investigate the fundamental validity of the Schottky emission model for its applications to electron injection into dielectrics from a metal or semiconductor electrode. We cover a wide range of electric fields from10kV/cm to 10MV/cm and a temperature span for a large range of barrier heights. We conclude the Schottky emission model is only applicable for a very small class of dielectrics under 0.1MV/cm and at high temperatures over ~330°K. For many defective dielectrics with a barrier height ($\Phi_B \geq$ 1eV) in BEOL/MOL/MIMCAP applications, the corresponding electric fields for the measurable currents far exceed 0.1MV/cm and up to 10MV/cm, the application of the Schottky emission model is unequivocally invalid so that the extracted barrier height values are fundamentally incorrect. Several misconceptions and malpractices as widely occurred in the reliability community have been clarified with a guide to avoid future misapplications.

10A - Authors' Corner

Thursday, March 31, 12:30 p.m. – 12:50 p.m. CDT

10B – Intro
Thursday, March 31, 10:45 a.m. – 10:50 a.m. CDT

10B - GaN (GaN Power Device)
Thursday, March 31, 10:50 a.m. – 12:30 p.m. CDT
Venue: International III & IV

10:50 a.m.
10B.1 - Modeling Hot-Electron Trapping in GaN-Based HEMTs, Nicola Modolo, Carlo De Santi, Gaudenzio Meneghesso, Enrico Zanoni, Matteo Meneghini; Department of Information Engineering, University of Padova, via Gradenigo 6/B, 35131 Padova, Andrea Minetto, Luca Sayadi, Sebastien Sicre, Gerhard Prechtl; Infineon Technologies Austria, Siemensstraße 2, 9500 Villach

Hot electron trapping can significantly impact the performance of GaN-based HEMTs. Within this paper, the effect of current density and electric field on the severity of hot electron degradation is presented. The experiments demonstrate that: (i) we can isolate the hot electron trapping processes, (ii) the hot- electron induced performance degradation follows a logarithmic kinetic, which can be modeled by rate equations, and (iii) the amount of current collapse has a linear dependence on the applied electric field and a logarithmic dependence on the current density, in agreement with theoretical equations.

11:15 a.m.
10B.2 - Gate Reliability of p-GaN Power HEMTs under Pulsed Stress Condition, M. Millesimo, E. Sangiorgi, C. Fiegna, A. N. Tallarico; ARCES-DEI, University of Bologna, Cesena, B. Bakeroot, Centre for Microsystems Technology, imec and Ghent University, M. Borga, N. Posthuma, S. Decoutere; imec - Kapeldreef 75, 3001 Leuven

A combined experimental/simulation analysis has been performed to study the gate reliability of GaN-HEMTs with p-type gate under pulse stress conditions. Results show that the time-dependent gate breakdown (TDGB) can be determined by two factors: i) the total ON-time during which the device is subjected to a positive gate bias before the failure; ii) the number of pulses, hence the number of switching phases from OFF- to ON-State and vice versa. The severity of the degradation ascribed to transition phases depends on the OFFtime (t_{OFF}) and transition time ($t_{TR} = t_{RISE} = t_{FALL}$). In particular, the shorter t_{OFF} and t_{TR}, the higher the Schottky junction voltage drop and the current peak during the switching phase, respectively. The higher voltage drop is ascribed to the semifloating potential of the p-GaN layer.

11:40 a.m.
10B.3 - Novel High Voltage Bias Temperature Instabilities (HV-BTI) Setup to Monitor RON/VTH Drift of GaN-on-Si E-Mode MOSc-HEMTs under High Drain Voltage, C. Leurquin, W.Vandendaele, A.G Viey, R. Gwoziecki, R. Escoffier, R. Salot, G. Despesse; Silicon Component Department (DCOS), Université Grenoble Alpes, F. Iucolano, R. Modica, A. Constant; Research and Development Department, STMicroelectronics

In this paper, we propose a novel characterization methodology to study dynamic R_{ON} and V_{TH} during a high voltage stress on the drain node of GaN-on-Si E-mode MOSc-HEMTs using a half-bridge configuration circuit and specific gate voltage waveforms. This novel setup enables to study simultaneously R_{ON} and V_{TH} during stress and recovery phases from 10µs to several kiloseconds. At 150°C a high carbon concentration in Carbon-doped GaN layer, reduces ON- Resistance degradation. Temperature dependent measurements show that R_{ON} degradation is related to C_N acceptor traps in the GaN:C layer. High voltage drain stress induces a combination of V_{TH} drift and access region related dynamic R_{ON} effect.

12:05 p.m.
10B.4 - GaN MIS-HEMTs in Repetitive Overvoltage Switching: Parametric Shift and Recovery, Qihao

Song, Joseph P. Kozak, Yunwei Ma, Jingcun Liu, Ruizhe Zhang, Yuhao Zhang; Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Roman Volkov, Daniel Sherman, Kurt V. Smith; VisIC Technologies, Ness-Ziona, Wataru Saito; Research Institute for Applied Mechanics, Kyushu University

The overvoltage and surge energy robustness of GaN power high-electron-mobility transistors (HEMTs) is a key gap recently identified by the JEDEC JC-70.1 committee. This work presents the first study on the parametric shift and recovery of an industrial depletion-mode metal-insulator-semiconductor HEMT (MIS-HEMT) in repetitive overvoltage switching close to its dynamic breakdown voltage. In each switching cycle, a voltage overshoot of up to 90% of dynamic breakdown voltage was applied during the device turn-OFF process. As the repetitive switching prolongs, the device showed shifts in threshold voltage, saturation current, and on-resistance, and these parametric shifts saturated after 1-million cycles. These parametric shifts are believed to be induced by the trapping of the holes generated in the impact ionization. After the repetitive switching, the device exhibited slow recovery in the natural state, at elevated temperatures, or with negative gate biases, due to the difficulty in hole removal. By contrast, applying a positive gate bias or a positive substrate bias can facilitate the hole migration towards the two-dimensional-gas (2DEG) channel for recombination, and therefore, accelerated the device recovery. In particular, a 50-V substrate bias allowed the device to recover in a few minutes. This work shows the good overvoltage robustness of GaN MIS- HEMTs and unveils effective methods for their post-switching recovery, as well as suggests the significance of hole dynamics for the device overvoltage switching close to the dynamic breakdown voltage.

10B - Authors' Corner
Thursday, March 31, 12:30 p.m. – 12:50 p.m. CDT

10C – Intro
Thursday, March 31, 10:45 a.m. – 10:50 a.m. CDT

10C - FA (Failure Analysis)
Thursday, March 31, 10:50 a.m. – 12:30 p.m. CDT
Venue: Cap Rock I, II & III

10:50 a.m.
10C.1 (Invited) - Putting AI To Work: A Practical and Simple Application to Improve 3D X-ray FA, William Harris, Allen Gu, Masako Terada; Carl Zeiss - Research Microscopy Solutions Dublin

This paper presents the demonstration of a deep learning-based reconstruction approach for working with 3D X-ray tomography/microscopy data, focusing on improving workflows in microelectronics failure analysis and reliability applications. Whereas the industry-standard filtered back projection (known as FDK) method of X-ray tomography reconstruction has been used for many years due to its simplicity and robustness, it has constrained the results of 3D X-ray scanning in terms of both image quality and scan speed. Powered by artificial intelligence technologies, the new deep learning high resolution reconstruction (DLHRR) approach discussed here offers broad improvements across diverse sample types including microelectronics, increases scan speed by a factor of 4X or more, is as easy to use as FDK without requirement for a machine learning expert, and is implemented on a desktop workstation PC. Results will be shown on IC packages and commercial battery devices.

11:15 a.m.
10C.2 - Defect-Controlled Resistance Degradation of Sputtered Lead Zirconate Titanate Thin Films, Kuan-Ting Ho, Daniel Monteiro Diniz Reis; Engineering Sensor Process Technology, Robert Bosch GmbH, Reutlingen, Karla Hiller; Center for Microtechnologies, Technical University Chemnitz, Chemnitz

Oxygen vacancy migration and lead vacancy hole trapping were identified in sputtered lead zirconate titanate thin film by thermally stimulated depolarization current measurement and charge-based deep level transient spectroscopy. The oxygen and lead vacancy were correlated to the first and second wave of resistance degradation, respectively, by the wafer-level process nonuniformity in both electric field polarities, which gives

alternatives to process assessment. The concentration of both defects can be controlled by process variations, and the resulting resistance degradation can be modelled using Schottky-limited conduction and two independent defect contributions.

11:40 a.m.
10C.3 - Power Cycling Reliability of SiC MOSFETs in Discrete and Module Packages, I. Kovacevic-Badstuebner, S. Race, T. Ziemann, S. Tiwari, U. Grossner; Advanced Power Semiconductor Laboratory, ETH Zurich, Elena Mengotti, Enea Bianda; ABB Switzerland Ltd., Corporate Research Center, Joni Jormanainen; ABB Drives Oy, Helsinki

This paper presents an analysis of power cycling (PC) capabilities of two industry-standard packages with silicon carbide power MOSFET dies: the discrete TO-247 package and a base-plate-less power module with silicone gel encapsulation. PC experiments show a more than an order of magnitude higher number of cycles to failure for the TO-247. The significant spread in the PC lifetime of TO-packaged SiC power MOSFETs by different manufacturers is correlated with die thickness, bond wire diameter, and number of bond wires. A failure analysis and electro-thermo-mechanical simulations point out that shorter PC lifetime in the case of power modules is due to a high stress in solder, while in the case of TO-packages it is ascribed to wire lift-off. The simulations indicate that rather than die thickness, the wire diameter is a critical parameter influencing wire lift-off.

12:05 p.m.
10C.4 - Progressive Degradation without Physical Failure During Mounting Due to Soft Overstress in Compound HBT for RF, Mobile, and Automotive Applications, Hyeokjae Lee, Sanggi Ko, Ho-Joon Suh, Gina Jeong, Jung-Han Yeo, Hye-Min Park, Hee-Kyeong Kim, Jong-Kwan Kim, Sung S. Chung, Youngboo Kim; QRT Inc., 109 Gwanggyo-ro, Yeongtong-gu, Suwon-si, Gyeonggi-do 16229, Jisun Park, Hyungsoon Shin; Ewha Womans University, 52 Ewhayeodae-gil, Seodaemun-gu, Seoul 03760

For the first time, we systematically analyzed the cause of gain degradation without physical damage in discrete III-V device and clarified that the cause was overstress during componentization. In order to reproduce no physical failure condition, medium-level pulse ESD/EOS voltages or TLP currents were zapped at MMIC. Through TCAD simulation, the part of performance degradation and the cause of the modeled degradation mechanism were analyzed together. It was also confirmed that the heat generation position matched the EMMI heating position using TCAD. Meanwhile, after checking the problematic point using EMMI, DC current was applied to weak point, and quasi physical failure point was also secured using FIB. We identified soft overstress and reproduced gain drop with no damage and isolated the weak position of HBT in discrete device with EMMI, and TCAD.

10C - Authors' Corner
Thursday, March 31, 12:30 p.m. – 12:50 p.m. CDT

Break
Thursday, March 31, 12:50 p.m. – 01:50 p.m. CDT

11A – Intro
Thursday, March 31, 01:50 p.m. – 01:55 p.m. CDT

11A - GD (Gate/MOL Dielectrics)
Thursday, March 31, 01:55 p.m. – 04:00 p.m. CDT
Venue: International I & II

01:55 p.m.
11A.1 - Middle-of-the-Line Reliability Characterization of Recessed-Diffusion-Contact Adopted sub-5nm Logic Technology, Seongkyung Kim, Ukjin Jung, Seungjin Choo, Kihyun Choi, Taejin Chung, Shinyoung

Chung, Euncheol Lee; Samsung Foundry Business, Samsung Electronics, Juhun Park, Deokhan Bae, Myungyoon Um; Samsung Foundry Business, Samsung Electronics

In this paper, we report middle-of-the-line (MOL) reliability characterization of recessed-diffusion-contacts adopted sub-5nm logic technology. The intrinsic MOL reliability including voltage-ramp-to-breakdown (Vramp) and time-dependent-dielectric-breakdown (TDDB) shows a notable improvement. MOL breakdown voltage (Vbd) is also comparable when a gate contact is placed next to a recessed-diffusion-contact. MOL Vramp related process parameters, such as critical dimension and height, are explained. MOL Vbd as an early diagnosis tool for process maturity, such as contact misalignment and dynamic voltage screening (DVS), on sub-5nm logic technology is addressed.

02:20 p.m.
11A.2 - On Superior Hot Carrier Robustness of Dynamically-Doped Field-Effect-Transistors, Stanislav Tyaginov; imec, Leuven 3001 & A.F. Ioffe Physical-Technical Institute, Russian Academy of Sciences, Aryan Afzalian, Alexander Makarov, Geert Hellings, Alexander Grill; imec, Leuven 3001, Michiel Vandemaele; KU Leuven, Department of Electrical Engineering (ESAT), Maksim Cherenev, Mikhail Vexler, Ben Kaczer; imec, Leuven 3001

We simulate relative changes of the saturation drain current during hot-carrier degradation (HCD) in dynamically-doped **(D_2)** and "traditional" planar complementary metal-oxide- semiconductor (CMOS) field-effect-transistors (FETs) of gate lengths and doping profiles. To achieve this goal, we use our physics-based model for HCD validated against experimental data from a broad range of transistor architectures (which include but are not limited to planar, fin, and nanowire FETs). These simulations show that at lower gate voltages of $\mathbf{V_{gs} \leq 0.9}$ V (i.e. covering the operating regime) $\mathbf{D_2}$ FETs have superior HC reliability compared to their CMOS counterparts, while at $\mathbf{V_{gs} \geq 1.0}$ V the CMOS FET begins to be more reliable (at shorter stress times, however, the **D2** device is still superior). Under these low stress voltages, HCD is governed by the multiple-carrier process of bond dissociation controlled by the carrier concentration (rather than energy), which has different $\mathbf{V_{gs}}$ dependences in **D2** and CMOS FETs. Based on conducted calculations, we suggest that, in addition to better performance and scalability compared to the CMOS counterpart, the **D2** FET has also superior hot-carrier reliability.

02:45 p.m.
11A.3 - New Modelling Off-State TDDB for 130nm to 28nm CMOS Nodes, Tidjani Garba-Seybou; STMicroelectronics, 850 Rue Jean Monnet & ISEN-REER, IM2NP UMR 7334, Place G. Pompidou, Xavier Federspiel, Florian Cacho; STMicroelectronics, 850 Rue Jean Monnet, Alain Bravaix; ISEN-REER, IM2NP UMR 7334, Place G. Pompidou

We present a detailed analysis of Off-state Time Dependent Dielectric Breakdown (TDDB) under non-uniform field performed in MOSFET devices from 28nm FDSOI, 65nm SOI to 130nm nodes. Oxide breakdown in thin gate oxide is characterized under DC stress with different gate-length LG and as function of drain voltage VDS and temperature. We show that the leakage current is a better monitor for TDDB dependence under Off-mode stress whereas a new modeling is proposed. It is found that Weibull slopes β are higher in PFET due large amount of injected hot electrons than in NFET when hot holes are involved.

03:10 p.m.
11A.4 - AC TDDB Analysis for HK/IL Gate Stack Breakdown and Frequency-Dependent Oxygen Vacancy Trap Generation in Advanced Node FinFET Devices by SILC Spectrum Methodology, P. S. Chen, Y. W. Lee, D. S. Huang, S. C. Chen, C. F. Cheng, J. H. Lee, Jun He; Advanced Technology Quality & Reliability Division, Taiwan Semiconductor Manufacturing Company

Be closer to real product operation, DC TDDB stress convert to AC TDDB could be one choice to wrestle with advanced node shrink limitation. The physical explanation of AC TDDB improvement is successfully interpreted through the analysis of oxide trap generation with HK/IL gate stack in advanced node FinFET technology using SILC spectrum methodology. It is found that AC TDDB improvement is due to more charge de-trap. NMOS

show less shallow and deep electron trap generation on HK and PMOS show less hole trap generation on IL during AC waveform transition.

03:35 p.m.
11A.5 (Late News) - Deep Cryogenic Temperature TDDB in 45-nm PDSOI N-Channel FETs for Quantum Computing Applications, Asifa Amin, Aarti Rathi, Sujit K. Singh, Abhisek Dixit; Department of Electrical Engineering, Indian Institute of Technology, Oscar H. Gonzalez, P. Srinivasan, Fernando Guarin; Quality and Reliability Engineering, GLOBALFOUNDRIES Inc.

We have investigated and report here for the first time time-dependent dielectric breakdown (TDDB) in 45-nm RFSOI n-channel floating body MOSFETs at cryogenic temperatures. DC constant voltage stress is applied at the gate while the substrate chuck temperature is varied from 300K down to 10K. While t63 decreases with increasing temperature, shape parameter β shows an inverted U-shaped behavior which is explained using the bandgap model. Three levels of activation energy are seen for high, low and deep low temperatures where the activation energy decreases from high to deep low temperatures. The observed behavior is further explained using carrier energy shift in the bandgap as per the percolation theory.

11A - Authors' Corner
Thursday, March 31, 04:00 p.m. – 04:20 p.m. CDT

11B – Intro
Thursday, March 31, 01:50 p.m. – 01:55 p.m. CDT

11B - RF (RF/mmW/5G)
Thursday, March 31, 01:55 p.m. – 04:00 p.m. CDT
Venue: International III & IV

01:55 p.m.
11B.1 (Invited) - 6G Roadmap for Semiconductor Technologies: Challenges and Advances, N. Cahoon, P. Srinivasan, F. Guarin; Globalfoundries US Inc, 400 Stone Break Road Extension, Malta NY

The sub-THz spectrum between 100GHz and 300GHz is of great interest for achieving next generation 6G cellular network goals of ultra-high data rate, ultra-low latency and high sensing precision. Carrier frequencies >100GHz create significant challenges, including higher losses, lower semiconductor device performance, and a smaller per element physical area that constrains circuit size, integration, power and thermal management. Semiconductor technologies with transistor performance >500GHz are needed for improved efficiency, gain, noise and area at the front end of the 6G phased array radio. Advances in SiGe BiCMOS have the potential to increase silicon transistor performance while leveraging the cost and scale of mature high-volume silicon manufacturing for 6G sub-THz. Compound semiconductor technologies such as InP and GaN have the best front end performance at sub-THz. Advances in heterogeneous and monolithic integration with silicon are needed to address the cost and scale concerns of high frequency InP and GaN. A comprehensive approach to reliability is essential in order to extract maximum performance without sacrificing reliability.

02:20 p.m.
11B.2 - Interpretation and Modelling of Dynamic-RON Kinetics in GaN-on-Si HEMTs for mmWave Applications, V. Putcha, H. Yu, J. Franco, S. Yadav, A. Alian, U. Peralagu, N. Collaert; imec, Kapeldreef 75, Heverlee, B. Parvais; imec, Kapeldreef 75, Heverlee & Vrije Universiteit Brussels, Belgium

This work shows that the complex dynamic-R_{ON} characteristics observed for scaled GaN HEMT devices results from the similar capture/emission activation energies of the defects present in different epitaxial layers. This work also (i) presents an optimized experimental scheme for a detailed analysis of the different charge-trapping mechanisms in GaN-on-Si HEMTs, (ii) describes the charge-trapping kinetics over a wide range of temperatures

using capture/emission time (CET) maps, and (iii) models the defect energy distribution in the AlGaN barrier by analytically deriving the 2D potential profile in the access region and combining it with the results from CET maps.

02:45 p.m.
11B.3 - Fe-Traps Influence on Time-Dependent Breakdown Voltage in 0.1-µm GaN HEMTs for 5G Applications, Marcello Cioni, Nicolò Zagni, Alessandro Chini; Dipartimento di Ingegneria "Enzo Ferrari", University of Modena and Reggio Emilia

Scaled (L_G = 0.1 µm) GaN HEMT technology is currently pursued for high-frequency applications (such as 5G), requiring high current/speed and blocking capability. However, traps introduced with intentional Fe doping yield time-dependent breakdown voltage (V_{BR}), seriously affecting reliability. Here, we investigate the role of Fe traps by pulsed I-V characterization performed at different pulse durations (T_{OFF}). A T_{oFF}-dependent V_{BR} is observed on tested devices and is ascribed to the time- dependent occupancy of deep acceptors in the buffer layer. More specifically, the decrease in V_{BR} for short pulses is attributed to the increased leakage due to the reduced ionization of Fe-traps. This interpretation is supported by 2D numerical simulations.

03:10 p.m.
11B.4 - GaN RF HEMT Reliability: Impact of Device Processing on I-V Curve Stability and Current Collapse, F. Chiocchetta, C. De Santi, F. Rampazzo, K. Mukherjee, A. Gerosa, G. Meneghesso, E. Zanoni, M. Meneghini; University of Padova, Department of Information Engineering, Jan Grünenpütt, Daniel Sommer, Hervé Blanck, Benoit Lambert; UMS - United Monolithic Semiconductors

We present an extensive analysis of the impact of passivation and gate foot etching on the reliability and trapping behavior of gallium nitride HEMTs for RF applications. The study is based on high-temperature reverse bias (HTRB) experiments and temperature-dependent drain current transient analysis. Three wafers are analyzed, differing in gate foot etching and passivation. We demonstrate that: (i) gate foot etching and passivation significantly impact on the stability of the gate-leakage characteristics during HTRB stress; (ii) best stability is obtained through the use of low pressure chemical vapor deposition (LPCVD); (iii) current transient measurements reveal the presence of two trapping processes, E1 and E2. While E1 is found to be semiconductor-related, the time constant of trap E2 strongly depends on the processing parameters and significantly increases in presence of optimized gate-foot etch and passivation. The results presented in this paper provide information for the optimization of advanced GaN RF devices.

03:35 p.m.
11B.5 (Invited) - DC and RF Reliability Assessment of 5G-MMW Capable GaN HEMT Process, Satyaki Ganguly, Kyle M. Bothe, Alexandre Niyonzima, Thomas Smith, Yueying Liu, Jeremy Fisher, Fabian Radulescu, Donald A. Gajewski, Scott T. Sheppard, Jim W. Milligan, Basim Noori, John W. Palmour; Wolfspeed, Inc., Durham, NC 27703

Owing to its high power, high efficiency, high gain and high frequency capabilities RF-GaN technology has not only dominated satellite, aerospace and telecom industry but also been tapped as the most promising candidate for 5G technology extension to millimeter wave (MMW) applications. Excellent device performances with output power density (Pout) exceeding 3 W/mm and peak power added efficiency (PAE) above 35 % have been demonstrated by Wolfspeed's 5G-MMW capable 28 V, 150-nm gate length (V5) GaN on SiC technology. In this work we show the comprehensive DC (both on and off state) and RF reliability assessment and lifetime projection (both DC and RF) of such MMW capable 28 V rated 150-nm gate length process technology (G28V5). The on-state and off-state results coupled with the reliability without hermiticity (RWOH) capability and intrinsic reliability assessment up to 31.5 GHz demonstrate the maturity and reliability of V5 technology as a true candidate for MMW applications.

11B - Authors' Corner
Thursday, March 31, 04:00 p.m. – 04:20 p.m. CDT

11C – Intro
Thursday, March 31, 01:50 p.m. – 01:55 p.m. CDT

11C - CR (Circuit Reliability and Aging)
Thursday, March 31, 01:55 p.m. – 04:00 p.m. CDT
Venue: Cap Rock I, II & III

01:55 p.m.
11C.1 (Invited) - Exploring Fault Injection Attack Resilience of Secure IC Chips, Makoto Nagata; Graduate School of Science, Technology, and Innovation, Kobe University, 1-1 Rokkodai

Fault injections and attacks on an integrated circuit (IC) chip using a variety of physical measures are reviewed. Laser fault injection (LFI) is highlighted for the essential vulnerability on the backside of an IC chip in flip-chip packaging. On-chip voltage waveform monitoring characterizes the voltage peaks induced by LFI and establishes the detection scheme against LFI attacks. The backside buried metal (BBM) technique is deployed by preventive measures for shielding from laser exposure, for avoidance and also waring of invasive laser attacks. The alleviation of backside LFI is proven by Si experiments with on-chip waveform monitoring.

02:20 p.m.
11C.2 - A Ring-Oscillator-Based Degradation Monitor Concept with Tamper Detection Capability, Javier Diaz-Fortuny, Pablo Saraza-Canflanca, Erik Bury, Ben Kaczer, Robin Degraeve; imec, Kapeldreef 75, 3001 Leuven, Michiel Vandemaele; imec, Kapeldreef 75, 3001 Leuven & ESAT, KU Leuven, Kasteelpark Arenberg 10, 3001 Leuven

Refurbished chips (i.e., chips re-used legally in circular economy) and counterfeited chips (i.e., used chips fraudulently sold as new) are a growing concern for the industry because of their poor reliability. In this context, various solutions for the detection of such chips have been presented in the literature, several of which make use of performance degradation detection circuits. In this work, we propose a new concept for a degradation monitor, which can (1) obtain the age of the chip and (2) detect if the chip has been tampered through high- temperature annealing. To demonstrate the principles of this concept, we designed a novel and versatile array of addressable ring-oscillators (ROs), a type of circuit that has been widely proposed to detect fraudulently recycled chips. The array IC was manufactured in a 28 nm CMOS technology and utilized as a reliability test vehicle. Using this chip, we performed an extensive study of degradation phenomena that affect the ROs, as well as the recovery that they undergo after the stress application has ceased. Finally, we examined the impact that temperature annealing has on the recovery of circuit degradation, thus fraudulently concealing prior usage of the chip.

02:45 p.m.
11C.3 - Efficient Evaluation of the Time-Dependent Threshold Voltage Distribution Due to NBTI Stress using Transistor Arrays, Christian Bogner; Institute for Microelectronics & Infineon Technologies AG, Tibor Grasser, Michael Waltl; Institute for Microelectronics, Hans Reisinger, Christian Schlünder; Infineon Technologies AG

For the design of reliable ICs the application of accurate transistor aging models is indispensable. However, especially for modern deeply-scaled technologies modeling NBTI induced aging poses significant challenges as transistors can not be characterized individually but need to be described as a statistical ensemble. We make use of a dedicated array structure enabling the collection of a large data-set at reasonable experimental time. Note that by using an extensive data-set the statistical confidence can be maximized. We present a modeling approach based on physical considerations to describe the aging of SRAM-sized transistors under consideration of statistical effects. Our approach applies a modified defect- centric model under consideration of RTN to describe the time-dependent V_{th} distribution. Furthermore, we introduce a simple method to extract parameters describing the distribution. Additionally, we show that our approach provides great flexibility regarding stress conditions as

well as scalability to different transistor dimensions, which makes it ideal for applications such as circuit simulation.

03:10 p.m.
11C.4 - Layer-to-Layer Endurance Variation of 3D NAND, Md Raquibuzzaman, Aleksandar Milenkovic, Biswajit Ray; Electrical and Computer Engineering Department, The University of Alabama in Huntsville, Md Mehedi Hasan, Department of Computer Science, Stony Brook University

The block size of flash memory chips has increased significantly with the introduction of 3D NAND technology, causing "big-block" management issues in storage systems. In this paper, we characterize endurance of individual pages in a block and show that pages in the bottom and top layers exhibit lower endurance than pages in the middle layers. This variation in endurance among pages can cause severe underutilization of big memory blocks. We find that erase threshold voltage (F_t) variation between the layers is the root cause for the observed endurance variation.

11C - Authors' Corner
Thursday, March 31, 04:00 p.m. – 04:20 p.m. CDT

Closing Ceremony, Prize Drawing & 2023 Introduction
Thursday, March 31, 04:20 p.m. – 04:35 p.m. CDT
Venue: International III & IV