Unified Approach for Simulation of Statistical Reliability in Nanoscale CMOS Transistors from Devices to Circuits

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Abstract

The scaling down of the CMOS transistors necessitates the adoption of Reliability-Aware circuits and systems design methodology. Indeed, charge trapping related issues such as random telegraph noise (RTN) and bias temperature instabilities (BTI) are major threats to SRAM yield and endurance. It is well understood that the interplay between statistical variability, introduced by the discreteness of charge and granularity of matter, and the discrete oxide charge trapping related degradation in transistors necessitates the interpretation of their performance- and reliability-figures of merit as time dependent stochastic variables. Corroborated by a surge of new experimental evidences an important paradigm shift has identified the discrete charge trapping/de-trapping in the gate oxide as unique phenomenon underlying both RTN and BTI. In this tutorial we will present the recent advances in the simulation of statistical variability effects from device to circuit level. The simulations are based on 3-D Kinetic Monte Carlo simulations technology that follow trapping/de-trapping history of large ensembles of microscopically different transistors, accounting for the discrete nature of both doping and oxide traps and reproducing the stochastic process ruling the discrete charge injection into the gate oxide. The results of the physical simulation of the time dependent evolution of the statistical variability are then captured in accurate time dependent statistical compact models. As a result accurate statistical circuit simulation can trace the statistical impact of the degradation on the functionality of the underlying circuits and systems. This allows the concepts of Design-Technology Co-Optimization (DTCO) to be extended into the reliability domain. We will illustrate the above comprehensive simulation approach with examples of statistical reliability simulations in contemporary and future bulk and FDSOI MOSFETs and FinFETs. We will use statistical SRAM simulation to illustrate how the results of the physical simulations can be used to evaluate the resilience of the corresponding SRAM circuits and to reduce the design margins.

About the Author

Asen Asenov (FIEEE, FRSE) is a founder and CEO of Gold Standard Simulations (GSS) Ltd. (www.goldstandardsimulations.com). GSS is the leader in physical simulation of statistical variability, statistical compact model extraction and generation technology and statistical circuit simulation. The GSS customers include foundries, IDMs, fables companies and design IP startups. Asenov is also a Director of SureCore, Ltd, a green SRAM design IP start-up company. As a James Watt Professor in Electrical Engineering and Leader of the 30 members strong Glasgow Device Modelling Group (http://web.eng.gla.ac.uk/groups/devmod/) Asenov directs the development of 2D and 3D quantum mechanical, Monte Carlo and classical device simulators and their application in the design of advanced and novel CMOS devices. Asenov has more than 690 publications and more than 170 invited talks in the above areas.