Session Co-Chairs: Yung-Huei Lee, TSMC, James Stathis, IBM
Regency Main
8:00 a.m. - Session Introduction

8:05 a.m.
5A.1
Physical Mechanism of Progressive Breakdown in Gate Oxides (Invited), F. Palumbo, S. Lombardo* and M. Eizenberg, Technion, *CNR-IMM

The dielectric breakdown of ultra-thin gate oxides for CMOS is reviewed. We discuss silicon devices with SiOxNy or high-k and poly-Si or metal gate, and then III-Vs with high-k/metal gate. A model on the breakdown growth dependence on voltage, temperature, oxide thickness, etc., is eventually discussed and compared to data.

8:35 a.m.
5A.2
Spectroscopy of SILC Trap Locations and Spatial Correlation Study of Percolation Path in the High-K and Interfacial Layer, N. Raghavan, M. Bosman* and K.L. Pey, Singapore University of Technology and Design (SUTD), *A*STAR

We propose a new methodology to estimate the location of the percolation (breakdown) path separately in the HK and the IL along transistor channel, making use of our unique TDDB test algorithm that enables us to separate the breakdown process into two sequential stages – initial breakdown of the interfacial SiOx(IL) layer followed by subsequent breakdown of the high-k. Results reveal high correlation of breakdown path between high-K and IL, although exceptions are still observed.

9:00 a.m.
5A.3

Oxide defects have been shown to be volatile, meaning that they can be deactivated and re-activated at the same site. In addition, these defects can transform and change their properties. We employ time-dependent defect spectroscopy (TDDS) to study these changes. Our findings suggest that these changes are ubiquitous and must be an essential aspect of our understanding of oxide defects. We finally suggest hydrogen-defect interactions consistent with our observations.

9:25 a.m.
5A.4

We use the TDDS to study single-traps contributing to PBTI in nano-scale high-k n-channel FinFETs. We found electron traps located in the HfO2, consistent with previous reports on stress-induced leakage
currents (SILC) and electron and hole traps in the SiO₂. The distributions of the discrete steps in ΔV_{th} induced by the traps are bi-modal for n-channel transistors. We demonstrated that the step height alone does not allow for a determination of the defect location.

10:10 a.m.


TDDB under positive gate voltage in nMOS Devices is studied. First, a stress interruption effect is evidenced on TBD and shown to depend significantly on fabrication process. Then, based on experiments done both with the OTF monitoring methodology and the Fast measurement using Agilent B1530A, the interruption signature on MOS parameters are analyzed. Finally, Maxwell-Wagner instability followed by dielectric relaxation mechanism is found to be responsible for the stress interruption effect on TDDB nMOS.

10:35 a.m.


For the first time, a new TDDB lifetime model is proposed to predict lifetime for AC inverter-like stress in FinFET device. The AC lifetime is governed by four mechanisms, including voltage switching, e⁻ detrapping, HCI and h⁺ injection. Among them, voltage switching and e⁻ detrapping improve TDDB lifetime; while HCI and h⁺ injection degrade the lifetime.

10:55 a.m.


We develop a detailed admittance model and a practical capacitor ac admittance based characterization methodology for border traps in Ge/III-V MOS. We show the relationship of border trap density derived from ac admittance measurements with BTI (Bias Temperature Instability). The conductance from capacitor admittance measurements can be used as an indicator for BTI reliability.

Session 5B – Memory

Session Co-Chairs: Chandra Mouli, Micron, Shosuke Fujii, Toshiba
Regency IV
8:00 a.m. - Session Introduction

8:05 a.m.

5B.1 Scaling and Write Error Rate of Perpendicular Spin Torque MRAM (Invited), D. Worledge, IBM Research
Spin torque MRAM is an emerging memory technology that possesses a unique combination of speed, density, endurance, and non-volatility. This talk will give a brief overview of Spin Torque MRAM. I will then describe the IBM group’s demonstration of reliable, high speed spin torque writing using new perpendicular magnetic materials that we discovered, including results on scaling down to 15 nm. Particular attention will be paid to failure mechanisms, including the intrinsic write error rate.

8:35 a.m.
5B.2  
Monte Carlo Model of Reset Stochastics and Failure Rate Estimation of Read Disturb Mechanism in HfOx RRAM, N. Raghavan, D. Frey*, M. Bosman** and K.L. Pey, Singapore University of Technology and Design (SUTD), *Massachusetts Institute of Technology (MIT), **A*STAR Institute of Materials Research and Engineering (IMRE)

In this study, we develop a percolation based framework to model the filament configuration in low resistance state (LRS) and a Kinetic Monte Carlo (KMC) routine to simulate gradual evolution of the filament during reset phase. The proposed model enables us to predict the statistical spread of disturb voltage ($V_{DIST}$), observe bimodal configuration of conductive filaments and estimate the failure probability of disturb events ($F_{DIST}$), accounting for their dependence on SET compliance and ramp rate.

9:00 a.m.
5B.3  

This work shows a comprehensive study of pulsed-operated variability and endurance in HfOx-RRAM. We analysed the dependence of switching variability on operation current, voltage and pulse-width, providing guidelines to optimize set/reset distributions in oxide RRAM for the first time. We then discuss the impact of current, voltage and pulse-width on cycling endurance. The results are explained by a new physics-based model for endurance controlled by defect injection from the bottom electrode during reset.

9:25 a.m.
5B.4  

Instead of fluctuating R-distribution of ReRAM, the non-fluctuating parameters of filament diameter and packing factor were adopted to describe ReRAM. A quantitative method of characterizing the filament diameter and packing factor of ReRAM has been developed for the first time. Moreover, a new prediction method for ReRAM data retention has been developed based on filament diameter and packing factor. Our model provides a method of accurately predicting the data retention distribution for high-reliability ReRAM production.

10:10 a.m.
5B.5  
A Microscopic Physical Description of RTN Current Fluctuations in HfOx RRAM, F.M. Puglisi, L. Vandelli, L. Larcher, A. Padovani, M. Bertocchi and P. Pavan, Università di Modena e Reggio Emilia

We explore the microscopic mechanisms generating RTN in RRAM through physical simulations. While MP-TAT at oxygen vacancies assists the charge transport, the slow time scale associated with RTN
fluctuations invokes the occurrence of different mechanisms. Kinetic Monte-Carlo simulations showed that RTN may result by the Coulomb interaction of O vacancies with “slow” interstitial oxygen located nearby, or by possible metastable states in O vacancy defects.

10:35 a.m.

5B.6

**Phase-Change Memory: Feasibility of Reliable Multilevel-cell Storage and Retention at Elevated Temperatures**, M. Stanisavljevic, A. Athmanathan, N. Papandreou, H. Pozidis and E. Eleftheriou, IBM Research – Zurich

In phase-change memory (PCM) MLC storage is seriously hampered by the phenomenon of resistance drift and the impact of temperature. Drift and temperature resilience is achieved using a specific non-resistance-based cell-state metric. The comparison of conventional resistance and a new enhanced (eM) metric demonstrates for the first time that reliable 2 bits/cell storage and subsequent data retention can be achieved in PCM cell arrays in the presence of temperature variation of 50 °C magnitude.

10:55 a.m.

5B.7


The impact of P/E cycling on the read current fluctuation of 65nm NOR Flash memories is studied. Experimental results show that discernible transition between RTN and 1/f noise can be detected at the initial phase of the cycling (<100 cycles), depending on the gate bias voltage. As cycles increase, the transition phenomena disappear and 1/f noise dominates. The phenomena are interpreted by the spectroscopy analysis of process and stress induced traps.

Session 5C - Chip Packaging Reliability

Session Co-Chairs: Alan Lucero, Intel, Christine Hau-Reige, Qualcomm

Big Sur II

8:00 a.m. - Session Introduction

8:05 a.m.

5C.1

**Probabilistic Design for Reliability in Electronics and Photonics: Role, Attributes, Challenges (Invited)**, E. Suhir and A. Bensoussan*, Portland State University, *Institute of Technological Research (IRT)

The recently suggested probabilistic design for reliability (PdFR) concept is based on highly focused and highly cost-effective failure oriented accelerated testing (FOAT), simple and physically meaningful predictive modeling (PM), and on FOAT and PM based sensitivity analysis (SA) methodologies is addressed. The PdFR analysis enables one also to check if the product is not "over-engineered", i.e., is not superfluously robust. The major PdFR concepts are illustrated by practical examples.

8:35 a.m.

5C.2
The Electromigration Behavior of Copper Pillars for Different Current Directions and Pillar shapes, C. Hau-Riege, R. Kumar, Y.Y. Sun, A. Bao, M. Shah, L. Zhao, O. Bchir, Y.-W. Yau, A. Syed, S. Bezuk and K. Caffey, Qualcomm Inc.

The electromigration (EM) performance of the copper pillars in our study is robust for die-side electron source, but vulnerable to the opposite electron flow direction. By testing structures with different Cu trace widths and pillar shapes, it was observed that the substrate-side electron source leads to extensive intermetallic compounds at the expense of the Cu trace as well as EM-voiding, which is exacerbated by narrower trace widths but improved by an oblong pillar shape.

9:00 a.m.
5C.3

This paper describes the critical importance of interfacial strength between copper lines and cap layer for catastrophic failure under chip package interaction (CPI). Chip package interaction (CPI) is an old and new issue. In this paper, base on our previous experimental results, we try to simulate the initiation and propagation of failure in interconnect structures and discuss the scenario for catastrophic failure under CPI.

9:25 a.m.
5C.4
Semi-Empirical Stress-based Acceleration of Temperature Cycling Failure, D. Huitink and A. Lucero, Intel Corporation

Packaging reliability acceleration models are important for predicting failure during a product’s life. However, qualification requirements are based on models from historical trends that are parameterized by extrinsic factors like temperature range. As new materials and packaging configurations drive new failure modes, it is important that acceleration is parameterized on intrinsic factors like stress/strain and energy to accurately extrapolate failure rates. This work proposes an acceleration model for thermomechanical cycling based on intrinsic accelerating factors.

10:10 a.m.
5C.5

The necessity of the Metal-Insulator-Metal Capacitor (MIMCAP) devices that helps electrical performance of integrated circuit (IC) has drastically increased for high performance mobile SoC applications. In this paper, a finite element analysis (FEA) of strain and stress analysis modeling and the benefits to electromagnetic interference for the MIMCAP embedded C4 package will be disscused from design and reliability perspectives. and will show superb EMI characteristics with ondie MIMCAP.

10:35 a.m.
5C.6
This paper reports the die thinning impact on trigate transistor devices performance due to package imposed stress through board attach. Results show that PMOS drive current increases while NMOS drive current decreases with reductions in die thickness. The impact of die over-mold thickness on the transistor shifts is also investigated and demonstrates the importance of considering such factors in establishing the correct balance between transistor performance impact and other characteristics such as package warpage.

THURSDAY AFTERNOON
April 23, 2015

Session 6A - Circuit Aging/Circuit Reliability

Session Co-Chairs: Keith Green, Texas Instruments, Barry Linder, IBM
Regency Main
1:20 p.m. - Session Introduction

1:25 p.m.
6A.1
Non-volatile Memory as Hardware Synapse in Neuromorphic Computing: A First Look at Reliability Issues (Invited), R. Shelby, G. Burr, I. Boybat and C. di Nolfo, IBM Almaden Research Center

A three-layer perceptron neural network with 164,885 synapses, in which each synapse strength is encoded by two phase-change memory (PCM) devices achieved a training accuracy of 82.2% and generalization accuracy of 82.9% for handwritten digit recognition, using a backpropagation algorithm suitable for non-volatile memory + selector crossbar array synapses. Modeling with a neural network simulator allowed extensive tolerancing with respect to PCM variability, yield, and conductance response.

1:50 p.m.
6A.2

Long-term BTI field data from IBM z systems in 32nm HKMG technology are obtained using a built-in monitor capable of separating the PBTI and the NBTI. The BTI monitor is paired with thermal sensor in proximity to correlate the BTI degradation with temperature. Comparable PBTI and NBTI degradation in use condition were observed. Compared with previous z microprocessor with 45nm SiON CMOS technology, the new 32nm microprocessor showed more than 2X reduction in BTI degradation.

2:15 p.m.
6A.3

The frequency shift due to fast Bias Temperature Instability (BTI) stress-recovery effects under Dynamic Voltage and Frequency Scaled (DVFS) were measured using a high resolution revolving reference silicon odometer. For the first time, this design provides DVFS frequency shift measurement only in 1µs period after the supply transition. The test chip was implemented in a 65nm process. The frequency shift measurements were observed across different voltage supply, temperature, stress time duration, and supply ramp duration.

The impact of frequency dependents BTI and HCI in RO degradation through a wide frequency range are also investigated. It is found frequency dependence of RO degradation comes from nHCI effect and it appears only at high bias. Even if nHCI effect becomes notable at high bias, NBTI is still the dominant degradation of RO in sub-GHz range. So the degradation slope of RO can not reflect the dominant degradation mechanism of RO.


In this paper, we introduce the benefits of extended 6T SRAM characterization at wafer level during the technology development phase. This allows accurately assessing yield and modeling degradation behavior based on wafer level measurement, to project to package level High Temperature Operating Life (HTOL) condition, while separating intrinsic from extrinsic time zero and end-of-life failures.

SRAM Vmax Stability Considerations, D. Burnett, S. Balasubramanian, V. Joshi, S. Parihar, J. Higman and C. Weintraub, GLOBALFOUNDRIES

At sufficiently high Vdd, the SRAM stability can degrade and be worse than the stability margin at Vmin. Further, the bitcell stability at high Vdd is much more sensitive to other factors, like resistance variation, than at low Vdd. This paper highlights SRAM Vmax stability issues observed for a 28nm technology and the increased susceptibility of high performance (HP) FinFET SRAM cells for Vmax SRAM fails.

Session 6B - Product IC Reliability

Session Co-Chairs: You Wen Yau, Qualcomm, Sangwoo Pae, Samsung
Regency IV

1:20 p.m. - Session Introduction

1:25 p.m.

28nm UTBB FDSOI Product Reliability/Performance Trade-off Optimization Through Body bias Operation, P. Mora, X. Federspiel, F. Cacho, V. Huard and W. Arfaoui, STMicroelectronics

This paper demonstrates the advantage of body biasing to set the best reliability/performance trade-off of electronic products. First we review experiments performed on transistors, ring oscillators and CPU to quantify the impact of Vb on reliability and performances. Then, the full picture including power, speed and reliability is discussed to highlight the way to get optimized circuits for different activities. Finally, a unique dynamic management of performance and reliability can be achieved through body biasing.
1:50 p.m.

6B.2

We developed product-level reliability estimator for 20nm technology, which is estimating chip failure rate by combining FR from all the blocks and by considering Gox/MOL TDBB and EM, based on rigorous check by using EDA tools. It provides precise product-level reliability risk based on actual use conditions and provides more flexibility to designers and thus helps them to enhance performance and reduce area without over designing for reliability concern.

2:15 p.m.

6B.3
**From BTI Variability To Product Failure Rate: A Technology Scaling Perspective, V. Huard, D. Angot and F. Cacho, STMicroelectronics**

This paper proposes to highlight the reliability challenges related to the transistor scaling. Scaling laws will be derived for mean BTI degradation and variability. The large dataset will allow drawing conclusions on variability root cause. Second, failure rate model is derived by considering an inter-woven approach of fresh and aged variability. These two models are used to study the impact of the technology scaling on failure rates down to 7nm node under various design strategies.

3:00 p.m.

6B.4

We demonstrate a fast test methodology for logic chips to characterize the net degradation behavior. Our procedure utilizes critical path delay as an indirect monitor of threshold voltage increase. RVS is used to measure voltage acceleration and to characterize the degradation modes and critical paths. RVS can be combined with CVS to extract complete degradation parameters for lifetime prediction.

3:25 p.m.

6B.5
**CpK Approach for the Qualification of ECC-Designs with Single Bit Failures, G. Tempel, Infineon Technologies Dresden GmbH**

A qualification methodology for non-volatile memories with ECC-design is presented. The production capability can be concluded from the measured bit-failure rates of different failing modes. Finally a specific Cpk target of the bit failure rates can be set for passing or failing.

Session 6C - Compound/Optoelectronics

Session Co-Chairs: Denis Marcon, IMEC, Jungwoo Joh, Texas Instruments
Big Sur II
1:20 p.m. - Session Introduction

1:25 p.m.

6C.1
**Commercialization and Reliability of 600V GaN HEMTs (Invited), T. Kikkawa, Transphorm Japan**
The commercialization and reliability of the 600V GaN HEMT using Si-CMOS compatible 6-inch line will be demonstrated. Neither evaporation nor lift-off method is used. JEDEC qualification of cascode packages is shown. Excellent dynamic on-resistance data up to 1000 V is demonstrated with showing high breakdown voltage over 1500 V. Ultimately high speed GaN will significantly reduce the system size endemic in all areas of electricity conversion, ranging from PV inverters to electric vehicles.

1:50 p.m.

6C.2


Threshold voltage drifts induced by forward gate bias stress or positive bias temperature instabilities (PBTI) are a severe problem for GaN MIS-HEMTs. Conventional temperature dependent stress-recovery experiments are insufficient to obtained the thermal activation of stress and recovery processes independently. We present some technological implementations of resistive heater structures suitable for GaN devices and utilize them to evaluate the thermal activation behavior of ∆VTh drifts and estimate its life time behavior due to PBTI.

2:15 p.m.

6C.3

**Origin of Physical Degradation in AlGaN/GaN on Si High Electron Mobility Transistors under Reverse bias Stressing**, W.A. Sasangka, G.J. Syaranamual, C.L. Gan and C.V. Thompson, Singapore-MIT Alliance for Research and Technology

The role of threading dislocations on the pits formation of AlGaN/GaN/Si HEMTs is investigated. Upon stressing, ID-saturation decreases over time. The amount of ID-saturation degradation correlates well with the pits formation at the gate-edge, where the electric field is the highest. It is found that pits tend to nucleate at threading dislocations that have screw component, even when they are at locations away from the gate-edge. An explanation based on electrochemical oxidation model is proposed.

3:00 p.m.

6C.4


AlGaN/GaN MIS-HEMTs received significant attention because of their low gate leakage current. In order to have a high gate overdrive, the gate dielectric strength is one of the critical reliability issues. The parameters affecting the gate dielectric strength, especially the time dependent dielectric breakdown (TDDB), have not been studied in depth yet for recessed gate devices. In this paper, the forward TDDB evaluation was performed on devices with different recessed depths and different gate dielectric hicknesses.

3:25 p.m.

6C.5

**Positive-Bias Temperature Instability of GaN MOSFETs**, A. Guo and J. del Alamo, Massachusetts Institute of Technology
Threshold voltage ($V_T$) instability after high voltage stress is a great reliability and stability concern for GaN power switching applications. In this work, we use a simple GaN MOSFET structure and study the positive bias temperature instability (PBTI) of the oxide/GaN system. We examine two gate dielectrics: SiO$_2$ and a SiO$_2$/Al$_2$O$_3$ composite. $V_T$ shift is explained well by a combination of well-established models for oxide trap and interface state generation.

3:50 p.m.
6C.6
Instabilities of SiC MOSFETs During use Conditions and Following bias Temperature Stress, G. Pobegen and A. Krassnig, Kompetenssentrum für Automobil- und Industriebetrieb (KAJ) BmbH

We investigate lateral 4H-SiC MOSFETs after switches of the gate bias. We observe a logarithmic time dependence of the trapping of electrons into the gate oxide which has the same root cause as positive BTI. By varying the device temperature we observe a behavior which is consistent with the kinetics of processes with distributed activation energies. The distribution has two distinct peaks where especially the low-energy peak is heavily affected by nitrogen POA.