**TUESDAY MORNING**  
April 17, 2012

**Session 2A: Memory**

10:30 a.m.
Session Introduction

10:35 a.m.

The assessment of distributed-cycling activation energy for scaled technologies requires a careful control of experimental tests, preventing spurious effects: in particular, we report on the possibility for long gate-stresses to give rise to parasitic drifts, which add to the threshold-voltage loss during post-cycling bake. When the superposition of the two phenomena is taken into account, the effectiveness of distributed-cycling is fully confirmed at the 45nm NOR node.

11:00 a.m.
**2A.2 Impact of Program/Erase Stress Induced Hole Current on Data Retention Degradation for MONOS Memories**, S. Fujii, R. Fujitsuka, K. Sekine, H. Kusai, K. Sakuma, M. Koyama, Toshiba Corporation

In order to understand the mechanism for data retention of MONOS devices after Program/Erase cycling, we carefully examined change of SILC during cycling, including identification of carriers that constitute SILC. As a result, it is found that hole injection, rather than electron detrapping, causes data retention degradation after cycling. The hole SILC degrades data retention through hole trapping and subsequent recombination with stored electrons. Strong correlation between hole SILC and interface-states generated by cycling stress is also demonstrated.

11:25 a.m.
**2A.3 Reliability Study of Magnetic Tunnel Junction with Naturally Oxidized MgO Barrier**, C. Yoshida, T. Sugii, Low-power Electronics Association & Project

Dielectric breakdown characteristics of naturally oxidized MgO barriers were investigated using a time dependent dielectric breakdown (TDDB) technique. We found that there is significant stress polarity dependence in these characteristics, which is caused by unoxidized Mg metal left at the bottom interface of the oxidized barrier. We also found that the oxidized barrier has a comparable dielectric strength and can be a good alternative to the sputtered barrier.

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**Session 2B: Process Integration/3D/TSV**

10:35 a.m.
**2B.1 Copper Through Silicon Via (TSV) for 3D Integration (Invited)**, C. Kothandaraman, IBM Systems & Technology Group

Differential expansion mismatch between Cu and Si and high aspect ratios required for TSV pose unique challenges to the integration and reliability of Cu TSV. A novel TSV structure that successfully mitigates these concerns has been integrated into CMOS with high K/metal gates. Data from test structures demonstrate no ‘Cu pumping’ or other deleterious effects to neighbouring devices or interconnects. High performance embedded DRAMs were stacked to make 3D modules utilizing this TSV technology and 500 MHz operation with less than 1.5 ns latency was demonstrated showing no impact from TSV processing.

11:00 a.m.
**2B.2 Assembly Process Integration Challenges and Reliability Assessment of Multiple 28nm FPGA Assembled on a Large 65nm Passive Interposer (Invited)**, R. Chaware, K. Nagarajan, K. Ng, S.Y. Pai, Xilinx, Inc.
Stacked die packaging has been gaining traction in recent years due to cost and manufacturing issues associated transistor scaling. 3D die stacking architecture offers a unique combination of low power and high bandwidth per watt without increasing the cost significantly. For Xilinx’s FPGAs (Field Programmable Gate Array), due its repetitive and smart structures, stacked silicon integration (SSI) technology becomes a perfect fit to provide a cost effective solution to build large die with very high logic cell count. In the current configuration, four different 28nm FPGA die are connected to each other through a 65nm passive silicon interposer. Arrays of more than 10k micro-bumps (ubumps) stitch these four dies together through the silicon interposer. This paper describes the technical challenges associated with 3D integration of 100um thin interposer and FPGA die on to a package and stacked die package reliability.

The assembly test vehicle was comprised of 4-slices of 28nm chip mounted side by side on a 25 mm x31 mm 100um thick interposer with thousands of micro-bumps at 45um pitch. This top die and interposer stack was assembled on a 35mm x 35mm and 45mm x 45mm package with 180um pitch C4 bumps. Several assembly experiments were performed to compare performance of mass reflow assembly and thermo compression bonding assembly to join top FPGA die with ubumps. To understand the impact of substrate on assembly organic package and ceramic package were used in initial assembly evaluations. Assembly yield and reliability were used as two main criteria in deciding the best assembly process. Micro-bump resistance was monitored by Through Silicon Via (TSV) chains, Kelvin bump structure and daisy chains in order to check interconnect integrity after assembly and during reliability testing. After assembly evaluations, separate underfill screening design of experiment (DOE) was performed to choose the best underfill candidates for reliability evaluations. Results of those DOE will be discussed in this paper. Reliability evaluations were performed with best underfill candidates and parts were subjected to L4 preconditioning and -55°C to 125°C thermal cycling. Parts were subjected to extended thermal cycling, i.e. beyond 1000 cycles, to understand the other possible failure modes. Various failure modes observed during reliability evaluations will be discussed in this paper.

Assembly evaluations showed that the choice of the assembly process was strongly dependent on the die size, interposer design and interposer process. Choice of flux also affected the ubump assembly yield and underfill flow. Underfilling experiments confirmed that optimization of underfill process required optimization of dispense pattern, ubump parameters. Reliability evaluations showed that the reliability was affected by choice of underfill, interposer cleaning, and die thickness/package structure. One of the common failure modes was delamination between interposer and C4 underfill.

11:25 a.m.


The effect of thermal cycling, accelerated thermal storage and long-term storage at room temperature on the performance of FEOL devices integrated together with through silicon vias (TSVs) is studied. It is observed that storage at high temperatures increases the stress in the Si induced by the TSV while thermal cycling and long-term storage at room temperature decreases this stress. Theses stress variations are hypothesized to be attributed to creep of copper in the Si via.

11:50 a.m.

2B.4 Impact of Cu Diffusion from Cu Through-Silicon Via (TSV) on Device Reliability in 3-D LSIs Evaluated by Transient Capacitance Measurement, K. Lee, J. Bea, Y. Ohara, T. Fukushima, T. Tanaka, M. Koyanagi, Tohoku University

The influence of Cu contamination from Cu TSV on device reliability in the 3-D LSI was electrically characterized by transient-capacitance measurement. The capacitance-time (C-t) curves of the Ta/Cu trench capacitors with thin Ta barrier layer (10-nm at the surface)were severely degraded after the initial annealing at 300°C. The C-t curves with thick Ta layer (100-nm at the surface)exhibit no change after annealing up to 60min at 300°C, but it show significant degradation after annealing at 400°C. Thick vertical Ta layer shows poor barrier quality than thin planar Ta layer.

Session 2C: Compound/OptoElectronics
10:35 a.m.
2C.1 Reliability of AlGaN HEMTs (Invited), U. Mishra, University of California, Santa Barbara

Under the ONR DRIFT program a large amount of coordinated work from some of the best groups in the US and Europe has resulted in an unprecedented level of understanding of the degradation mechanisms in AlGaN/GaN HEMTs. The scope of the program is vast and so in this paper only some of the methodologies employed and outcomes of the research will be summarized.

11:00 a.m.

In this work we tested AlGaN/GaN HEMTs with off-state critical voltage >100V. We show that the on-state degradation of those devices can be unambiguously attributed to hot-electrons. In order to discriminate the degradation’s accelerating factors (temperature Tj, electric field, hot electrons or a combination), we carried out dc tests at constant dissipated power and at several VGS and VDS values (different electric field and hot electrons conditions).

11:25 a.m.
2C.3 Direct Correlation Between Specific Trap Formation and Electrical Stress-Induced Degradation in MBE-grown AlGaN/GaN HEMTs, A. Sasikumar, A. Arehart, S. Ringel, S. Kaun*, M. H. Wong*, U. Mishra*, J. Speck*, The Ohio State University, *University of California, Santa Barbara

DC stressing of molecular beam epitaxy (MBE)-grown high electron mobility transistors (HEMTs) is found to degrade device performance primarily due to increased defect/trap formation. Using constant drain-current deep level optical/transient spectroscopy (CL_{D}-DLOS/DLTS) methods, a specific virtual-gate related electron trap with energy E_{C}-0.45 eV was observed to increase in concentration following DC stressing. The enhanced formation of this defect correlates quantitatively with a stress induced knee-walkout (performance-degradation) of the HEMT that was determined using pulsed I-V Measurements.

11:50 a.m.
2C.4 Long Duration High Temperature Storage Test on GaN HEMTs, F. Vitobello, A. Barnes, European Space Agency

As part of a large reliability test campaign a long duration high temperature storage test has been performed on GaN HEMTs to identify diffusion or contact related failure mechanisms. The storage test has been performed for 7000 hours and 15000 hours at 330°C and 275°C respectively and the changes in electrical and physical properties analyzed.

TUESDAY AFTERNOON
April 17, 2012

Session 2D: Failure Analysis

2:00 pm
Session Introduction

2:05 p.m.
2D.1 Comparison of Applications of Laser Probing, Laser-Induced Circuit Perturbation and Photon Emission for Failure Analysis and Yield Enhancement (Invited), S. Kasapi, R. Ng, J. Liao, W. Lo, B. Cory, H. Marks, NVIDIA

The transparency of the silicon substrate in CMOS circuits to near infra-red light has enabled a rich variety of optical techniques for observing and modifying circuit behavior. The main classes of optical analysis techniques are photon emission, laser-induced circuit perturbation, and, more recently, laser probing. The innovations in laser probing present...
significant new opportunities for failure analysis and yield enhancement. This paper presents several case studies with particular emphasis on how the new laser probing techniques complement and extend the established approaches.

2:30 p.m.

This paper presents, for the first time, near-infrared spectral photon emission measurements of a ring oscillator in IBM’s 45 nm SOI process technology. The setup employs a cryogenic cooled MCT camera and different band-pass filters with a very broad spectral range from 850-2100 nm. The paper will present the spectral data, discuss the thermal contributions, and analyze its impact for selecting appropriate detectors and tools for time-resolved measurements in present and future technology nodes.

2:55 p.m.

A simple visualizing technique of diffusion regions at a specific area in sub-100 nm node CMOS devices was proposed using porous silicon phenomena. This technique can be applied for both NMOS transistors and PMOS transistors simultaneously. A failure with highly-resistive electrical characteristics in a 90 nm-node transistor was analyzed using this technique. As a result, it was revealed that the failure was caused by a local block of LDD ion implantation.

3:20 p.m.

For the first time, we observed the discrete distribution and fluctuation of active B dopants in scaled nFETs and in various B-doped epilayers by the site-specific scanning spreading resistance microscopy (SSRM), which may clarify the origin of the nFET-Vth fluctuation. The B fluctuation is attributed to B-dopant segregation, which depends on thermal diffusion and even occurs under thermal equivalent conditions without geographical stress. SSRM is proven to be capable of observing dopants in doped silicon.

4:05 p.m.
**2D.5 A Study of Junction Photocurrent Changes Caused by Defective Gate Oxide**, H.S. Lin, United Microelectronics Corporation, Ltd.

It has been widely revealed that AFM laser beam may induce photoperturbation and hence significantly deteriorate the characterization accuracy of AFM based tools. This paper gives direct evidence that the optical excitation process may yield the temporary source of minority carriers. By taking advantage of this non-negligible photoelectric effect, a novel approach which is likely to be used to evaluate gate oxide quality was developed. In this study, it was observed that defective gate oxide can cause junction photocurrent changes, or the junction photocurrent can be correlated to gate oxide quality.

4:30 p.m.

Pulsed Laser Assisted Chemical Etching (PLACE) is an advanced method of surface preparation for analytic investigations such as: Focused Ion Beam (FIB) circuit edit, Failure Analysis chemical processes (poly-Si etch), Backside SIMS and Optical techniques such as Photomission Microscopy. PLACE can achieve ultra-high purity and fine dimensional control since it is a dry process relying on pyrolytic vapor phase reactions initiated, and constrained, by a pulsed laser.

*Session 2E: Chip-Package Interaction*
2:05 p.m.


We will address package-induced degradation of BEOL structures and approaches for recovery. For dielectrics, we will cover process options for ULK films and how these lead to differences in strength. For metals, the package constraints drive integration in new directions. We will also address how CPI changes as feature size and layout evolve.

2:30 p.m.

2E.2 Low-k - Package Integration Challenges and Options for Reliability Qualification (Invited), A. Lucero, G. Yu, D. Huitink, Intel

Traditional packaging materials and reliability standards are evolving as low-k die – package integration challenges increase. Low-k dielectric constants of die interlayer dielectric (ILD) materials are expected to continue to reduce to manage Resistance/Capacitance delay as interconnect or cell geometries are reduced. Mechanical strength is also reduced with the improvement in dielectric constant. The scaling of mechanical strength properties must now be considered when designing packaging and selecting materials for packaging and assembly. Die-package integration challenges are most often observed when placing large die on flipchip packages where the differences of the coefficient of thermal expansion (CTE) between the package and die become more pronounced with larger die. In particular the underfill material and Si backend must be designed to mitigate the CTE difference by having adequate strength to carry or buffer the interfacial loads without exerting enough force to pull off the ILD or package films while at use temperatures. Properties like viscosity must also be managed for successful assembly processing. Underfill materials properties are typically coupled with the glass transition temperature, Tg, which means that the CTE and modulus properties that are required for use performance and reliability of the die-package system are fixed to a small range. Traditional reliability standard testing and requirements do no comprehend the new reality where CTE often follows below the traditional reliability stress test temperature. Alternatives proposed by JEDEC to insure the reliability in the use conditions have not yet been adopted by many parts of the industry resulting in false failures and risk assessments when the rel. test temperature ranges exceed the Tg of the materials. Fortunately there are many reliability characterization, analysis and reliability estimation methods that can be used to protect the end user. This talk summarizes the die-package integration challenges and trends that the industry is starting to experience along with options to select, evaluate and qualify reliable products.

2:55 p.m.


This paper targets describing a sensor based methodology for the characterization of 3D stacking and packaging steps with MOSFET transistors in the main focus. N-type FETs are justified as an optimal solution by means of electrical characterization, calibration to stress, FEM modeling and stress measurement tests.

3:20 p.m.

2E.4 Die-Package Stress Interaction Impact on Transistor Performance (Invited), G. Leatherman, J. Xu, J. Hicks B. Kilic, D. Pantuso, Intel Corporation

Shifts in transistor performance due to mechanical stress interaction of thin die packaging, test socketing, and board mount are discussed. Transistor drive current and Vt shifts, characterized using ring oscillators, vary significantly across die posing concerns for predictable circuit performance. Numerical models are developed that correlate well with data.

4:05 p.m.

2E.5 Electromigration Degradation Mechanism Analysis of SnAgCu Interconnects for eWLB Package, T. Frank, C. Chappaz, L. Arnaud, X. Federspiel, F. Colella, E. Petitprez, L. Anghel*, STMicroelectronics, *TIMA Laboratory
Electromigration of SnAgCu solder balls is studied. Technology is Fanout embedded Wafer Level Ball Grid Array. Black’s parameters regarding stage of degradation are analysed through approaches based on resistance slope modeling and on Failure Criterions (FC). First stage of degradation is found to be dominated by Intermetallic Compound (IMC) growth, whereas late stage, up to open of the structure, is dominated by the voiding occurring at RDL / solder interface.

4:30 p.m.
**2E.6 The Impact of 45 to 28nm Node-Scaling on the Electromigration of Flip-Chip Bumps**, C. Hau-Riege, Y.-W. Yau, L. Zhao, Qualcomm

We have studied the electromigration reliability for different UBM and PI sizes as well as plated Ni and sputtered Cu UBM thicknesses on lead-free flip-chip bumps. Results from different UBM sizes lead to $n = 1$, thereby suggesting a void-growth-limited failure mechanism, where Joule heating inflates this value to $\geq 2$. Also, thin plated Ni and sputtered Cu layers independently led to early fails, due to improper barrier coverage which allowed fast CuSn intermetallic transformation.

**Session 2F: Circuits Reliability**

2:05 p.m.

It is well known that circuits fail when one or more of the constituent components fails, due -for example- to phenomena such as electromigration in wires. Such “hard” failures, typically due to topological changes in circuit connectivity, are treated distinctly from “soft” failures which are due to components drifting out of spec due to aging. However, in certain types of circuits, such as SRAM, the distinction between soft and hard failures is not clearly defined. The primary cause of the blurring between these two phenomena is manufacturing variability, which can make a topologically correct circuit behave as if it had a short or an open. This paper will show the linkage between these two failure types, and show how increasing variability in future technologies will likely exacerbate this problem further.

2:30 p.m.

To develop a robust NBTI prediction method under excessive randomness, this work collects statistical device data from a 65nm test chip. By comparing model prediction from short-term stress data (20ks) with direct long-term measurement (200ks), we conclude that the degradation follows logarithmic dependence with time (derived from the trapping/detrapping mechanism) and correctly captures the aging variability due to the randomness in number of available traps, thereby accurately predicts mean and variance of Vth shift.

2:55 p.m.

A simple but powerful recovery model is calibrated with a wide set of stress sequences. The model implies less recoverable NBTI degradation as VDD is increased. The activity of the transistors inside a circuit becomes critical to understand the impact of recovery. The duty cycle and frequency trends are not sufficient to judge for the amount of circuit-level aging. Even the circuit topology contributes to the degradation, and therefore recovery should be analyzed carefully.

3:20 p.m.
In the development of MOSFETs first “Hot Carrier Injection” (HCI) played an important role for reliability aspects [1,2]. With new shrunked process generations and nitrided gate oxides additionally the „Bias Temperature Instability” (BTI) raised and became the most critical mechanism. Some publications even claim that HCI is negligible in main-stream applications [3-6]. But is this statement generally true or is it the result of a partial view? This paper will discuss the area of conflict regarding the importance of N/PBTI and HCI. Some typical examples will illuminate different fields of applications with one dominating damage mechanism. Specific characteristics of these circuits and operation conditions leading to an outbalance of HCI or Negative-/Positive-BTI will be carved out. Finally it will be evaluated if a general trend is observable.

4:05 p.m.

2F.5 Impact of Interconnect Length on BTI and HCI Induced Frequency Degradation, X. Wang, P. Jain, D. Jiao, C. Kim, University of Minnesota

The dependence of BTI- and HCI-induced aging on interconnect length has been examined for the first time. Based on measurement results from 65nm test chips and verified by our model, we found that BTI-induced aging decreases monotonically with longer wire because of the shorter stress time, while HCI-induced degradation has a non-monotonic relationship with interconnect length due to the combined effect of increased effective stress time and decreased effective stress voltage.

4:30 p.m.

2F.6 Usage-Based Degradation of SRAM Arrays Due to Bias Temperature Instability, A. Bansal, J.-J. Kim, R. Rao, IBM T.J. Watson Research Center

SRAM array stability degradation with time, due to BTI, is estimated by assuming either static stress (pessimistic) or alternating stress with 50% duty cycle (optimistic). During field usage of an SRAM array, degradation completely depends on the customer workload. We show a novel approach to estimate the usage based degradation of SRAM stability. Using our approach, one can accurately predict workload based EOL degradation of an SRAM array, and a realistic VMIN EOL guard band.