AC admittance and SILC measurement techniques are combined together to study 5 kinds of traps in FinFET's HK/IL gate stack (4 in HK and 1 in IL). The traps change dynamically, depending on the process conditions, types of MOS, stress temperature, and the recovery conditions. Shallow traps in HK are recoverable, while deeps traps in HK are permanent damages. After analyzing the trap evolution during TDDB stress, the researchers conclude that (i) IL traps are insignificant to the NMOS HK/IL breakdown, (ii) the deep traps in HK are responsible for NMOS breakdown, and (iii) the PMOS breakdown is caused by traps in IL and deep traps in HK.

Fig. A. By AC admittance and SLIC techniques, 5 types of traps (4 in HK and 1 in IL) are identified and studied during TDDB stress.

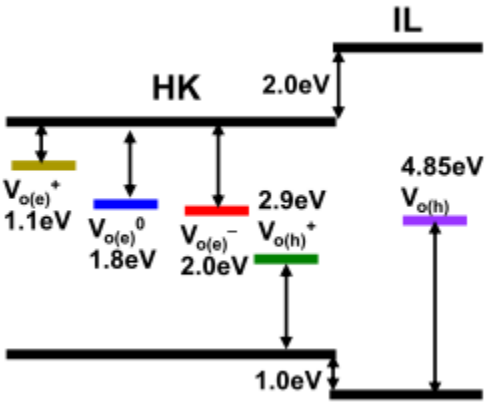

Fig. B. NMOS: Traps in IL is insignificant to the gate dielectric breakdown. The breakdown is due to the deep traps (Vo(e)0 and Vo(e)-) in HK. PMOS: HK/IL breakdown is caused by traps in IL (Vo(h)) and deep traps in HK (Vo(e)0 and Vo(e)-).