BTI reliability of a post-CMOS transistor based on 2D MoS2 semiconductor is investigated. MoS2 FETs using hexagonal boron nitride (hBN) have superior BTI reliability than MoS2 FETs using SiO2. Interestingly, charge trapping dynamics on MoS2/hBN and MoS2/SiO2 MOSFETs is found similar to that observed in conventional Si/SiO2 MOSFETs so the universal relaxation model, which is used on Si/SiO2 devices, can be applied to the MoS2 devices.

Fig. A. MoS2 FET devices using either SiO2, SiO2/hBN, or hBN as the gate dielectric are studied. The hysteresis width $\Delta V_H$ normalized by K =($V_{Gmax}$-$V_{Gmin}$)/dox, published in this work, is claimed smallest as compared with the literature results.

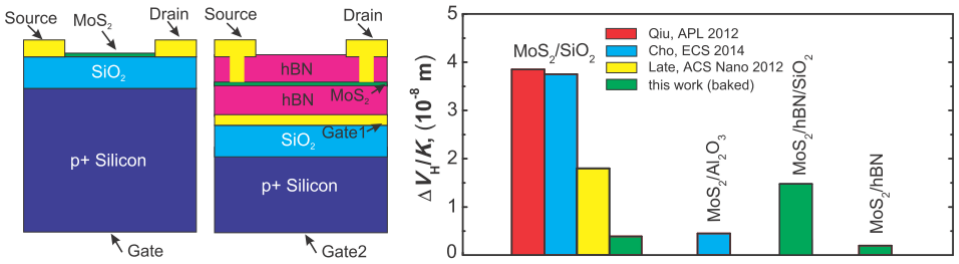


Fig. B (a) MoS2/hBN FETs show PBTI and NBTI degradation at elevated temperatures. (b) The degradation is recoverable when the stress is removed. Interestingly, both NBTI and PBTI on MoS2 devices can be fitted by the universal relaxation model from the Si/SiO2 MOSFETs. This suggests similar charge trapping dynamics on MoS2 devices.