FinFET technology greatly suppresses the SER (Soft Error Rate) to less than 20% of the planar counterpart's. 3B.4 presents extensive logic SER data across different flip-flop designs using state-of-the-art 14-nm FinFET process. The simulation reveals that SER increases when additional NMOS with smaller Qcrit (= 1.3 fC) is introduced. Reducing that NMOS area connected low Qcrit node can easily to attenuate alpha induced single event upset (SEU) FF rate.

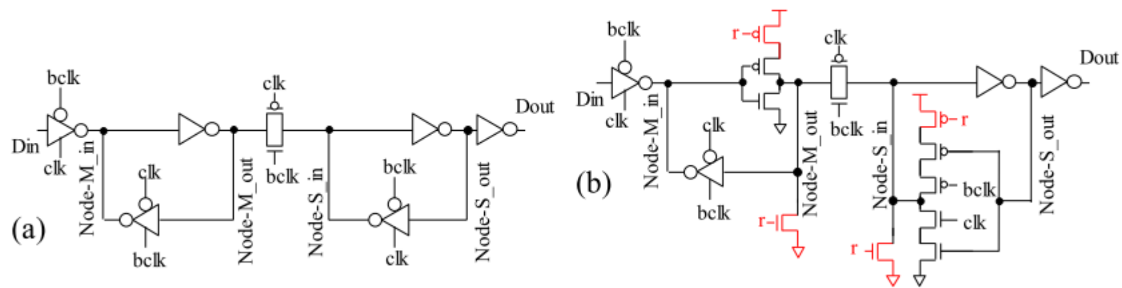

Fig. A. Schematic of (a) FF1 and (b) FF5. FF5 allows reset the flip-flop data by using additional NMOS (in read) and PMOS (in red).

Table I. Qcrit on 14 nm FinFET FF1 and FF5. The node name corresponds with the figure above. The SER increases from FF1 to FF5 because FF5 has additional NMOS in NODE-S_in (Qcrit = 1.3 fC). Note that Qcrit in 14 nm FinFET SRAM is 0.7 fC.

Node name	FF1	FF5
Node-M_in	1.3 fC	1.4 fC
Node-M_out	4.1 fC	3.6 fC
Node-S_in	1.3 fC	1.3 fC
Node-S_out	3.6 fC	3.8 fC