IRPS 2016 Tutorial Schedule

	Track 1: Technology Section F/G	Track 2: Component Section D	Track 3: System Section E
	Sunday Morning		
8:30 a.m. - 10:00 a.m.	Introduction to Reliability Physics and Engineering	MEMORY 1 – The Physics of Flash Memory Reliability	An Overview of Mechanical Reliability Challenges in Electronics Across Length Scales
	Joe McPherson - McPherson Reliability Consulting LLC	Riichiro Shirota / Hiroshi Watanabe - National Chiao Tung Univ.	Shankar Ganapathysubramanian and Sudarshan Rangaraj – Amazon Lab126
10:00 a.m. - 10:15 a.m.	Break		
10:15 a.m. - 11:45 a.m.	FEOL Reliability - From Dielectric Trap Properties to Degradation Mechanisms and Their Distributions	MEMORY 2 - Advanced Memory Technologies: CBRAM and OxRAM	
	Ben Kaczer and Robin Degraeve - imec	Shosuke Fujii - Toshiba Corp	
11:45 a.m. - 1:15 p.m.	Lunch		
	Sunday Afternoon		
1:15 p.m. - 2:45 p.m.	MOL Process Integration and Reliability Assessment Challenges	2.5D PACKAGING - Si Interposer, Heterogeneous Devices	Learning from and Reduction of IC Customer Returns
	Richard Southwick - IBM	Sam Gu - Qualcomm	Fred Kuper and Michael Stevens - NXP Semiconductors
2:45 p.m. - 3:00 p.m.	Break		
3:00 p.m. - 4:30 p.m.	BEOL Reliability - Challenges from Technology Scaling to Chip Design and System Integration	3D PACKAGING - Reliability of 3D Through-Silicon-Via (TSV) Technologies	SECURITY - What are the interactions between hardware reliability and system security?
	Baozhen Li - IBM	Dimitris P. Ioannou - GlobalFoundries	Swarup Bhunia - University of Florida
	Monday Morning		
8:30 a.m - 10:00 a.m	Wafer Level Reliability - Techniques and Models for Determining FEOL/BEOL Failure Mechanisms	CIRCUIT AGING 1 - Optimizing VLSI Circuit Reliability through Presilicon Design and Postsilicon Adaptation	Concepts for Managing System Behavior in the Presence of Hardware Faults
	Yung-Huei Lee - TSMC	Sachin S. Sapatnekar - University of Minnesota	Jim Lewis - Oracle America Inc
10:00 a.m - 10:15 a.m	Break		
10:15 a.m - 11:45 a.m	Challenges in Reliability Evaluations Due to FINFET Self-Heating Effects	CIRCUIT AGING 2 - Measurement Techniques	Soft Errors in Functional and System Safety Standards
	Steve Mittl - IBM	Takashi Sato and Hidetoshi Onodera - Kyoto University	Riccardo Mariani - Yogitech SpA
11:45 a.m - 12:45 p.m.	Lunch		
	Monday Afternoon		
12:45 p.m. - 2:15 p.m.	Failure Analysis Techniques	Reliability Differences Between RF and Power Switching GaN Power Transistors	ESD and EOS Design and Qualification Methods
	Kevin Johnson - Intel	Michael J Uren - University of Bristol	Charvaka Duvvury - Charvaka Duvvury LLC at ESD Consulting