Things are heating up at the

2017 IEEE International Reliability Physics Symposium (IRPS)

April 2-6, 2017
Hyatt Regency Monterey Resort and Spa, Monterey, CA, USA

The International Reliability Physics Symposium (IRPS) is the world's premier forum for leading-edge research addressing developments in the Reliability Physics of devices, materials, circuits, and products. IRPS is the conference where **emerging Reliability Physics challenges** and possible solutions to achieve realistic End-of-Life projections are first discussed.

The 2017 IRPS conference has been finalized with **19 tutorials**, **17 invited talks, 82 platform presentations**, and **81 posters** by a globally well-represented 145 technical program committee members and chairs. The **keynote speakers at IRPS 2017** will be **NASA Astronaut Dr. Nancy Currie-Gregg** "*Reflections on the risk of human space exploration – lessons learned from past failures*" and **IBM Distinguished Engineer Mr. Ronald Newhart**. Dr. Currie-Gregg, who flew on STS-57, STS-70, STS-88 (the first International Space Station assembly mission – 1998) and STS-109, will speak on NASA human exploration missions and reliability challenges. Mr. Newhart, who is currently a Distinguished Engineer with IBM Systems & Technology Group, focusing on product engineering and reliability, will give a keynote speech on system level reliability challenges with technology scaling, with details posted already on Facebook, LinkedIn and Twitter. The technical program will then commence with three parallel tracks; a listing of the accepted abstracts is posted with the program in review http://irps.org/program. The conference has 13 technical areas, which encompass the entire reliability area of semiconductors. Unique to this year's conference are focus areas of reliability testing methods, and the use of Commercial Off the Shelf (COTS) components in high reliability applications. In addition to these new topics, IRPS continues to be the premier venue in reporting emerging reliability concerns of Wide Band Gap semiconductors.

Why IRPS?

For 55 years, IRPS has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability. Drawing participants from the United States, Europe, Asia, and other parts of the world, IRPS is **the only comprehensive reliability conference covering the breadth of device reliability** from time dependent dielectric breakdown testing and models to compound device reliability to interconnect electromigration to soft error to electronic system reliability to process integration to chip-package interaction. No other meeting presents as much leading work in so many different areas of reliability of electronic devices, encompassing both silicon and non-silicon devices, process technology, packaging, circuits and systems reliability, photovoltaics, and MEMS. IRPS kicks off with two days of 90minute tutorials (http://irps.org/program/tutorials/) given by world-wide industrial and academic experts. The semiconductor reliability neophyte wonders where, how, and when to be trained most efficiently. The well-practiced engineer wants to stay current in their reliability training and become a little more broadened in other areas. A university professor or post doctorate wants perspective. An IEEE Fellow is great in their area, but seeking other areas to lead. Since 2011, IRPS conference has offered 129 x 90 minute sessions with an average of over 21 unique sessions per year delivered by industry, academia, and government experts. There is no other place to have this type of exposure and training. IRPS consists of three days (Tues-Thurs, April 4-6) of plenary and parallel technical sessions presenting original, state-of-the-art work. IRPS 2017 will also offer **tutorials**, **evening panel** debates and **workshops**, invited plenary talks, and an **outstanding technical program**.

Pre-Conference Highlights

Tutorials begin with one track covering "reliability fundamentals" in silicon: FEOL, BEOL, electro-migration, and chip-package interactions. The second track consists of wide bandgap (GaN), VLSI design methodology and verification, NAND flash memory, and failure analysis challenges with respect to reliability. The second day of tutorials consists of advanced topics in silicon, automotive-IOT, integrated/memories, and circuit & system reliability. The automotive-IOT track is a new focus area for IRPS with tutorials on functional safety relationship to reliability along with juggling knowledge and standards based qualification methods.

At the 2017 IRPS, there will be two entire sessions devoted to the reliability of **Wide bandgap (WBG) semiconductors** semiconductor devices one for SiC and one for GaN-based devices. **In the SiC tracks, 4 key speakers** have been invited to discuss about the reliability of today SiC MOSFET technology. These speakers will discuss and share their recent findings on threshold instabilities, design aspects for reliable high voltage operation, transient Out-of-SOA robustness and reality aspects of ultra-high voltage SiC MOSFETs. The GaN sessions focus mainly on **reliability aspects of GaN-based devices** for high voltage applications. In the GaN sessions, new reliability insights, understanding and aspects of GaN-based devices in cascode-mode, power GaN-based transistors under high (reverse) voltage stress and e-mode power devices are presented. Moreover, the GaN session includes also studies on the gate degradation of InAlN/AlN/GaN HEMT devices as well as the role of dislocations in carbon doped GaN buffers on Si.

The **transistor and beyond CMOS subcommittee** will have two sessions. In the first session, papers covering different aspects of BTI, HCI and self-heat effects will be discussed. Some aspects of variability will also be covered. In the second session, papers will cover some of the physical mechanisms of reliability, degradation of III-V channel transistors and also some reliability aspects of novel channel materials.

Recent advancements in **memory reliability** will also be showcased at IRPS, including process optimization for MRAM and for vertical NAND memories as well as system-level approaches for SSDs. The emerging memory field is also represented, with studies on RRAM variability and error recovery.

In the **dielectric session** it will demonstrated that Weibull distribution is insufficient to represent the complexities of FinFET degradation with solid statistical and physical evidence. The novelty lies in the unified understanding gained using physical analysis tools (HRTEM with EELS and EDX) and percolation framework based statistical derivation to justify the need for a clustering model. Also there will be the first reports probing the breakdown phenomenon in a few (2L/3L) layered fluorinated graphene (FG) stacks at sub-nanoscale resolution in ultra-high vacuum (UHV). Experimental evidence of stress induced degradation and breakdown (BD) at nanoscale, progressive shrinkage of bandgap and multimodal BD distributions will be presented at the symposium.

The **metallization reliability** session will present the recent investigation of novel interconnects for continuous scaling, that include a) Cobalt or Ruthenium-filled interconnects, b) doped Graphene-Nanoribbon (GNR) interconnect, c) new low-resistivity ALD-W capping, and d) atomically thin diffusion barriers. Also, there will be reports covering the effects of self-heating on electromigration and stress-migration, as self-heating becomes a limiting factor for semiconductor reliability.

The **Circuit Reliability/Aging** session includes innovative papers on a wide range of topics. A thermally aware aging sensor design implemented in a 20nm SoC illustrates the advantages of incorporating such sensors to bound FEOL aging without exceeding the power constraints. Further, a novel on-die wave-front generator circuit is used to generate realistic AC waveforms to stress transistors as they would be in actual high-speed I/O applications. Also, a Physically Unclonable Function (PUF) is

demonstrated by taking advantage of the intrinsic randomness of gate oxide breakdown position as the entropy source.

The **Product** session will cover the latest industry trends on qualification, advancing the discussion on how we'll ensure next generation technologies are comprehended at the product level. Platform and Poster presentations will span a variety of product segments, from Automotive to CPUs to FPGA and beyond.

The **packaging sessions** reflect recent industry trends toward scaling through the **package in 2.5/3D designs**. The session will feature reliability results from new package architectures accomplished using new applications of build-up processes as well as through interposers. The comparative reliability impact of a TSV-middle process on front-end of line (FEOL) devices and back-end of line (BEOL) structures will be presented. TSV orientation relative to fin-FET device orientation was studied. One comparative example shows the gate-oxide breakdown voltage (VBD) for thin and thick gate-oxide devices at a keep out zone (KOZ) distance of 3µm from the TSV compared to the reference devices.

Innovative findings on **soft errors** in advanced electronic devices will also be reported, in particular: i) new insight on back bias effect on SOI SRAMs soft error rate, ii) Pioneering results on Polonium-diffusion effect on alpha emission rate and related soft errors; iii) The re-emergence of thermal-neutron soft errors in 16-nm FinFETs and iv) Soft errors in 10-nm FinFETs. Furthermore an invited talk on autonomous driving, discussing the challenges of implementing a safe, secure, complex driver assistance system will complete the session.

The photovoltaic session shows innovative findings on reliability of organic and inorganic solar cells. Innovative modeling and characterization techniques for the polymeric solar cells, as new tools for comparing the reliability and performances of different materials, as well as a method for investigating the degradation mechanisms of organic solar cells will be discussed. The profound difference of behavior between forward and reverse bias stress on thin film silicon solar cells, showing a clear evidence of the range of wavelengths of the photons needed to assist the recovery effect under DC voltage stress will also be presented. The severe effects of potential-induced damage will also be reported, demonstrating that a significant number of PV modules installed are PID sensitive, and highlighting the importance to detect and recover the PID affected PV modules in an early stage in order to be able to recover them to an acceptable level.

The inaugural year of the **Reliability Testing session** will focus on the test equipment and methods that are used to design and perform modern reliability tests. Platform presentations will include topics ranging from product level reliability test concerns, to novel circuit level test structures, and device level defect detection using ultra high speed measurement. The practical aspects of testing will be explored along with the underlying physics of reliability.

Reliability of wide variety of systems will be presented at the **systems reliability** session. Systems will include mobile displays, Space systems with focus on commercial of the shelf (COTS) components, ceramic capacitors based systems, counterfeit electronics and semiconductor systems. In addition, two approaches will be presented to gather and assimilate data to improve reliability of systems. One approach is to gather telemetry data from the device in the field and guide the system design based on this data to to improve field reliability. Second approach is data-driven hybrid physics-based technique for reliability allocation in early product development stages such that more reliable products can be designed for the customer.

Other opportunities at the symposium include:

- **Year in Review** Session (Monday April 3). These seminars provide a summary of the past year's most noteworthy research and development in the field of microelectronics reliability. The distinguished speakers cull information from the recent literature and product announcements and provide an expert's interpretation of the impact. The Year in Review session helps the attendees to stay current with the recent reliability literature.

- **Evening Poster Session**. The poster session will provide an additional opportunity for authors to present their original research. The setting is informal and allows for easy discussion between authors and other attendees.

- **Evening Session Workshops.** These workshops enhance the symposium by providing the attendees an opportunity to meet in informal groups to discuss key reliability physics topics with the guidance of experienced moderators. All conference attendees are invited to join discussions of one or more of six topic areas, including self-heating effects on transistor reliability, expectations of extrinsic reliability in high reliability vs. low cost markets, middle of line dielectric models, GaN reliability testing, solid state drive reliability, and consumer off the shelf components in high reliability systems. These workshops provide excellent networking opportunities, as well as a forum for lively debate on the best approaches to characterizing and controlling reliability.

- **Vendor Exhibits**. Held in parallel with the technical sessions, the equipment demonstrations provide a forum for manufacturers of state-of-the-art laboratory equipment to present their products. Attendees are encouraged to visit the manufacturers' booths for information and demonstrations.

- **IRPS Paper Awards**. IRPS bestows awards for Best Paper, Outstanding Paper, Best Poster and Best Student Talk. The Best Paper author is typically invited to present the paper at ESREF in October.

The Conference center at the **Hyatt Regency Monterey Hotel and Spa** captures an atmosphere of intense energy and inspiration and has become a favored destination for corporate meetings, business retreats, training sessions and conferences.

Please take advantage of registration now for lower conference fees and follow us on Facebook, Linked-In, Twitter @IEEEIRPS, or visit http://IRPS.org for the latest information. We look forward to seeing you in Monterey!

Gaudenzio Meneghesso, Publicity Chair
University of Padova, Italy

Koji Eriguchi, Publicity Co-Chair – Asia
Kyoto University

Yuan Chen, General Chair
NASA.

Picture 1: Beautiful Monterey- a great place for a conference

Picture 2: Management Committee Meeting, December 2016. **Firts row from left**: Gaudenzio Menghesso (Publications & Publicity Chair), Mark Porter (Technical Program Chair), Charles Slayman (Audio Visual Chair), Cathy Christiansen (Workshops Chair), Yen-Hao Shih (Arrangements Chair). **Second row from left**: Koji Eriguchi (Publicity Co-Chair – Asia) Jason Ryan (Communications Chair & Secretary), Susumo Shuto (Registration Chair), Yuan Chen (General Chair), Chris Connor (Tutorials Chair), Robert Kaplar (Finance Chair), Vincent Huard (Presentations Chair), Christine Hau-Riege (TP Vice Chair)